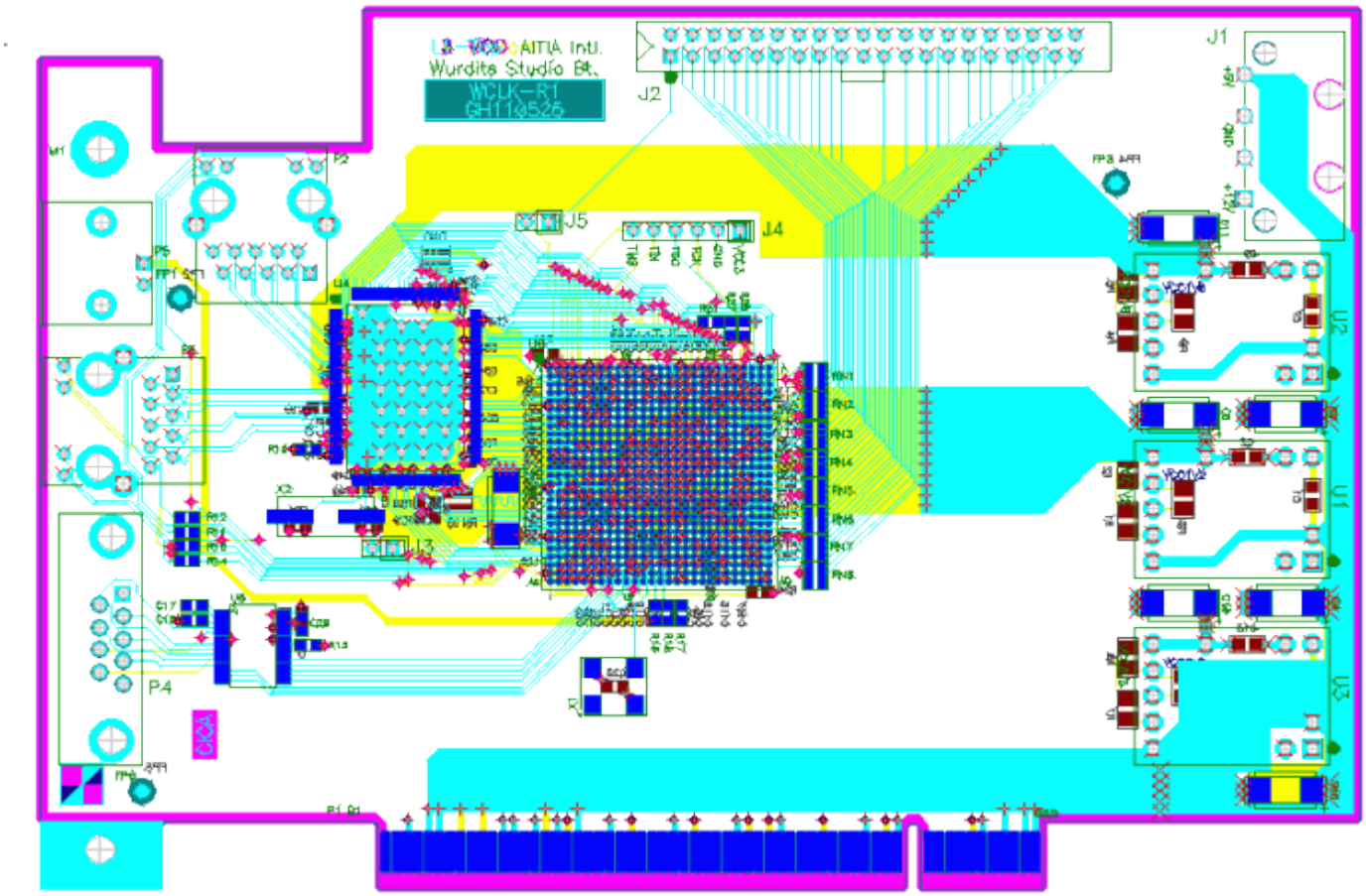
SGA-CLOCK

card

Wall Clock adapter for SGA series

network analyzers



REFERENCE MANUAL

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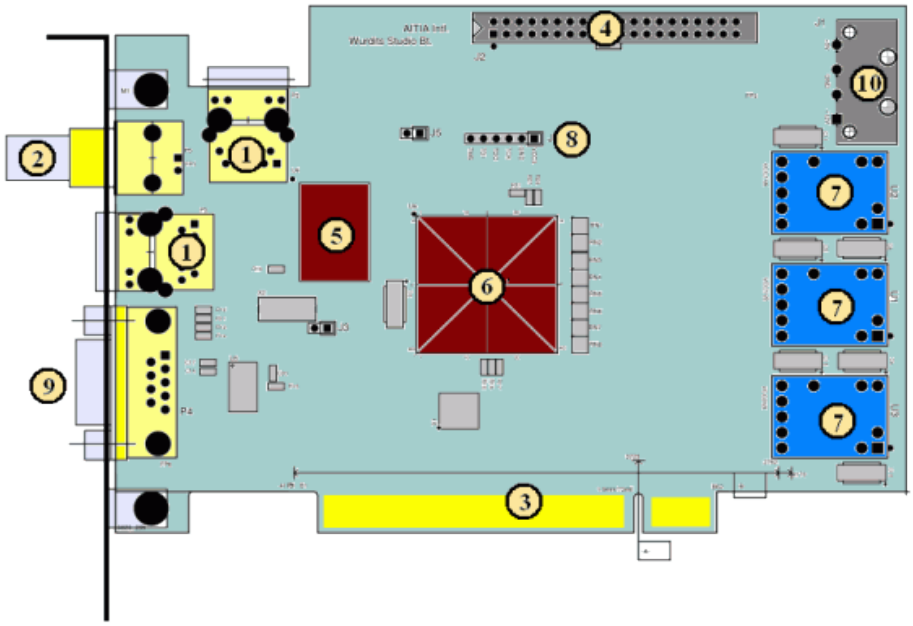
Contents

1.1 What is SGA-CLOCK?

SGA-Clock provides accurate wall clock and time-stamp services for SGA series network analyzer cards. It can lock to NTP servers and GPS based timing source and NMEA records as well as coventional G703 signals. It's on-board resources, and reconfigurability of its FPGA extends its functionality beyond the SGA application,

1.2 What is on-board?

The figures below show the major on-board components.



Top side components:

1: Dual 10/100/1000 Megabit/sec RJ45 receptacle	**6:** Xilinx Spartan 3AN family FPGA device
2: GPS PPS or G703 signal input	**7:** Switching regulators for 1.2, 1.8, and 3.3 Volts
3: PCI Connector feeding 12V power rail only	**8:** JTAG connector for programming the FPGA or Flash
4: 40 pin Berg type Feature Connector	**9:** RS232 interface (NMEA/console)
5: RTL8212 Dual 10/100/1000 Ethernet transceiver	**10:** PC style power connector

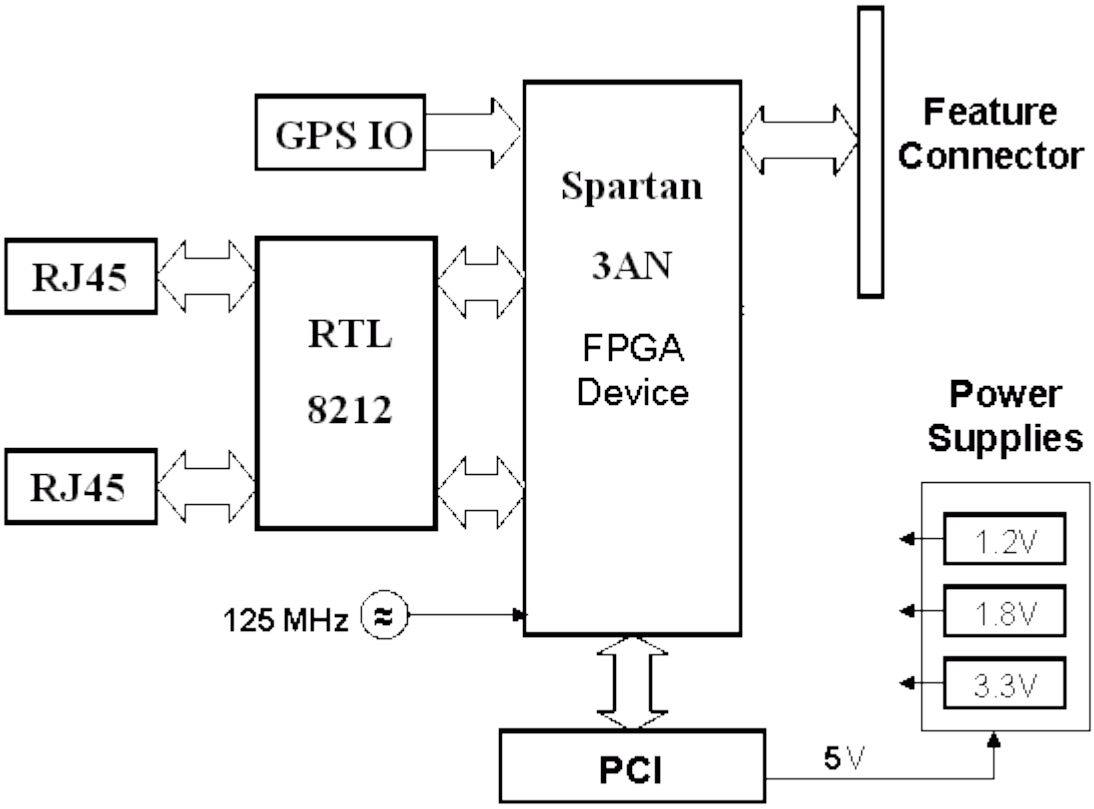
1.3 Conformity

SGA-Clock and its applications aim the following Standards/Recommendations:

Ethernet	**10/100/1000 Mbps Ethernet** IEEE Std 802.3 Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications
NMEA	**National Marine Electronics Association** “NMEA 0183 Standard For Interfacing Marine Electronic Devices,” Version 3.01, January 1, 2002
PCI	**PCI (form factor, power rail only)** PCI-SIG PCI Local Bus Specification Revision 2.2 December 18, 1998
FC	**40 pin Feature Connector**
...PDH	ITU-T G.703 Physical/electrical characteristics of hierarchical digital interfaces (.9 with passive feature card)
...HDD	NCITS 361-2002 AT Attachment with Packet Interface - 6 (ATA/ATAPI-6/UDMA5/UDMA100/UATA100 interface)

2. Architecture

The simple and robust architecture of SGA-Clock is shown on the block diagram below.



The heart of the board is a Xilinx Spartan-3AN family FPGA device.

- XC3S1400AN-FGG676-4 (for SGA-Clock board)

The main characteristics of the devices are shown in the table below:

	XC3S1400AN-FGG676-4
Array metric	82x144
Slices	11264
LUT RAM	176 kbits
Block RAM	576 kbits
Multipliers	32
DCM	8

2.1 Power Supply

The signal names, nominal voltages, maximum load current, and designated targets are the following:

Signal name	V	A	Targets	Notes
VCC1V2	1.2	10	FPGA, RTL8212	Core voltage
VCC1V8	1.8	3	RTL8212	Analog supply
VCC3V3	3.3	10	FPGA	I/O, AUX
	.	.	RTL8212	Analog

2.2 Clock sources

There are five clock sources available on SGA-Clock for the FPGA cores. The following tables shows their name, nominal frequencies, designated FPGA pins, and their application.

Signal	f [MHz]	FPGA#	Application
GTXCLK125	125.00	AE13	System/Global Clock
P1TXC	2.5/25	P4	Interface 1 TX clock
P1RXC	2.5/25/125	P2	Interface 1 RX clock
P0TXC	2.5/25	B13	Interface 0 TX clock
P0RXC	2.5/25/125	A14	Interface 0 RX clock
XTIO	25 5	R8	Central clocking output

Note that XTIO can be used to feed central clock to RTL8212. Close J3 jumper to override the crystal oscillator at X2.

2.3 RTL 8212 Dual Ethernet Transcevier

The SGA-Clock board has an RTL8212 tri mode (10/100/1000) Ethernet transceiver on board.

The table below lists the transceiver pins and the corresponding FPGA connectivity as well as MDIO and Status information for LED controls.

Signal (U4)	TRX#	FPGA#	Signal (U4)	TRX#	FPGA#
P0RXC	109	A14	P1RXC	62	P2
P0RXDV	107	C16	P1RXDV	60	V2
P0RXD[0]	106	B17	P1RXD[0]	59	Y2
P0RXD[1]	102	A18	P1RXD[1]	56	Y1
P0RXD[2]	102	A19	P1RXD[2]	55	AA2
P0RXD[3]	98	A20	P1RXD[3]	54	AC3
P0RXD[4]	97	C21	P1RXD[4]	52	AC2
P0RXD[5]	96	B21	P1RXD[5]	51	AB1
P0RXD[6]	94	B23	P1RXD[6]	49	AD2
P0RXD[7]	93	A22	P1RXD[7]	48	AD1
P0GTXC	117	A12	P1GTXC	69	L4
P0CRS	115	B15	P1CRS	65	R2
P0COL	114	A15	P1COL	64	R1
P0RXER	110	D17	P1RXER	63	U1
P0TXC	116	B13	P1TXC	68	P4
P0TXEN	118	A10	P1TXEN	70	K3
P0TXD[0]	120	A9	P1TXD[0]	72	J4
P0TXD[1]	121	A8	P1TXD[1]	73	H1
P0TXD[2]	122	B7	P1TXD[2]	75	H2
P0TXD[3]	123	B6	P1TXD[3]	76	G3
P0TXD[4]	124	B4	P1TXD[4]	78	E1
P0TXD[5]	135	A4	P1TXD[5]	79	D3
P0TXD[6]	126	B3	P1TXD[6]	80	B2
P0TXD[7]	127	A3	P1TXD[7]	91	B1
MDIO	128	C26	LEDDA	3	D26
MDC	1	C25	LEDCK	2	E26
RTRSTB	45	AD25			

2.4 PCI connector

The PCI connector (designated as P1 on-board) is used to feed 5V power supply.

2.5 Interface status LEDs

Network interface connectors have bult in magnetics, and status LEDS. Dual color LEDs can be controlled by decoding LEDDA and LEDCK signals. The table below contains the pinout of the dual color status LEDs.

Signal (on P2)	LED pin	FPGA#	Signal (on P3)	LED pin	FPGA#
M0DD1	Green+ Yellow-	AE3	M1DD1	Green+ Yellow-	AF5
M0DD2	Yellow+ Green-	AF3	M1DD2	Yellow+ Green-	AE6
M0DD3	Green+ Yellow-	AE4	M1DD3	Green+ Yellow-	AD7
M0DD4	Yellow+ Green-	AF4	M1DD4	Yellow+ Green-	AE7

2.6 Feature Connector

Mainly for historical reason, a 40 pins BERG type Feature Connector (designated as J5) is used for SGA-Clock.

The table below shows the pinout assignment for FPGA cores implementing **IDE/HDD** applications.

Signal (even)	J5#	FPGA#.	Signal (odd)	J5#	FPGA#
FRST	01	H14	GND	02	-
FD[7]	03	J14	FD[8]	04	H20
FD[6]	05	K14	FD[9]	06	J20
FD[5]	07	L14	FD[10]	08	L20
FD[4]	09	G15	FD[11]	10	J21
FD[3]	11	H15	FD[12]	12	K21
FD[2]	13	J15	FD[13]	14	L21
FD[1]	15	L15	FD[14]	16	G22
FD[0]	17	G16	FD[15]	18	H22
GND	19	-	FKEY	20	J22
FDRQ	21	J16	GND	22	-
FIOWN	23	K16	GND	24	-
FIORN	25	L16	GND	26	-
FIORDY	27	H17	FBALE	28	K22
FDACKN	29	J17	GND	30	-
FIRQ	31	H18	FIOCSN	32	G23
FA[1]	33	K18	GND	34	-
FA[0]	35	H19	FA[2]	36	H23
FCSN[0]	37	J19	FCSN[1]	38	L19
FACT	39	K19	GND	40	-

Note that FPGA reprogramming can be initiated from the feature connector. Closing J5 jumper allows FSRT signal to pull PROG pin low.

2.7 RS232 port/PPS input

A serial communicaton port is attached to SGA-Clock allowing direct console access through a DB9 connector at P4.

Normally it is used to receive NMEA records from a GPS device, in order to obtain wallclock - date/time.

Time stamp counters then can be locked to PPS input signal to achieve the highest accuracy.

The table below shows the pin assignment for the console port.

Signals	DB9 pin	FPGA#
C1DCD in	1	AE10
C1RXD in	2	AF9
C1TXD out	3	AF12
C1DTR out	4	AF10
C1DSR in	6	AE8
C1RTS out	7	AE12
C1CTS in	8	AF8
C1RI in	9	AE9
PPS Interface signals		
PPSIN in	AF14	
PPSTRM tri	AE14	

2.8 FPGA Programming

The Spartan 3AN family FPGAs have on chip flash PROM for configuration data. The configuration is automatic, although the FLASH and the FPGA can be programmed through the JTAG connector J4.

Since the FLASH is accessible from the FPGA, a properly crafted core can reprogram configuration data from the feature connector during an upgrade procedure.

3.1 Overview

SGA-Clock lays on a four layered FR4 PCB with SMD components on both sides, and gold plated edge connector. Through hole, and heavier componets are inserted on top.

Its form factor conforms the PCI, 3/4 Length Add-in Card with an I/O Bracket.

The following chapters describe the layer stacking, the metric of routing/plane copper layer, etc...

3.2 Layer stacking

The table below shows the layer structure of the board, and the names of the corresponding GERBER files.

1	17.5 um Cu	SGA-Clock_L1_top.gbr
	250 um prepreg	-
2	35 um Cu	SGA-Clock_L2_gnd.gbr
	1000 um Core	-
3	35 um Cu	SGA-Clock_L3_vcc.gbr
	250 um prepreg	-
4	17.5 um Cu	SGA-Clock_L4_bot.gbr

3.3 Metric

The narrowest traces are 6 (six) mils wide. The clearence (TT,TP) is 6 (six) mils.

Via's are all 'through' types, and covered by solder mask coating on both sides. All potential test points are available on SMD pads.

The Solder Mask Annual Ring is 2 mils (for Non-Solder-Mask-Defined pads too).

Smallest vias are 20/10 mils. All plane connections are direct type, for better cooling and conducting performance.