SGA C-GEP
100 Gbit/s Ethernet Evaluation Platform

Programmable, Multi-purpose Networking Platform

The system is built on a high performance **FPGA-based custom hardware** and a **firmware** that is **dedicated to network processing tasks**. The architecture focuses on the system-level integration of specified packet processors, integrated into one, high performance system.

The main purpose is to provide means for handling 1, 10, 40, and 100 Gbit/s Ethernet traffic in a flexible manner.

Application Areas

The architecture allows various networking applications for implementation. Thanks to the optimized firmware on its FPGA, it naturally handles the tasks of **SDN** (Software Defined Networking) Forwarding/Data plane. The **on-board Linux PC** can host the Control Plane functions for SDN, as well as various management tasks. When using other firmware on the FPGA, C-GEP can be applied as media gateway, traffic generator, or provide hardware-support for **DPI** (Deep Packet Inspection) tasks.

The Ultimate Monitoring Probe

C-GEP can be used as a monitoring probe for traffic measurements, since it provides **lossless** packet capture even at **100 Gbit/s** link speed. C-GEP is able to synchronize its high precision local clock (ns-resolution timestamp) with a **PTPv1** (IEEE 1588-2002) master device. The architecture can host an even more precise local source: the **SA.45s chip-scale atomic clock**.

Technical details

- High performance Virtex 6 FPGA (XC6VHX255T or XC6VHX380T)
  - GTH transceivers - 1x100 Gbit/s, 3x40 Gbit/s or 12x10 Gbit/s configurations
  - GTX transceivers - 20x1 Gbit/s, 5x10 Gbit/s configurations, other variations
- COM Express management PC connection to the FPGA via PCIexpress
- 2 x DDR3 slots for buffering and temporaly data storage
- USB, VGA, and fast Ethernet management port

AITIA

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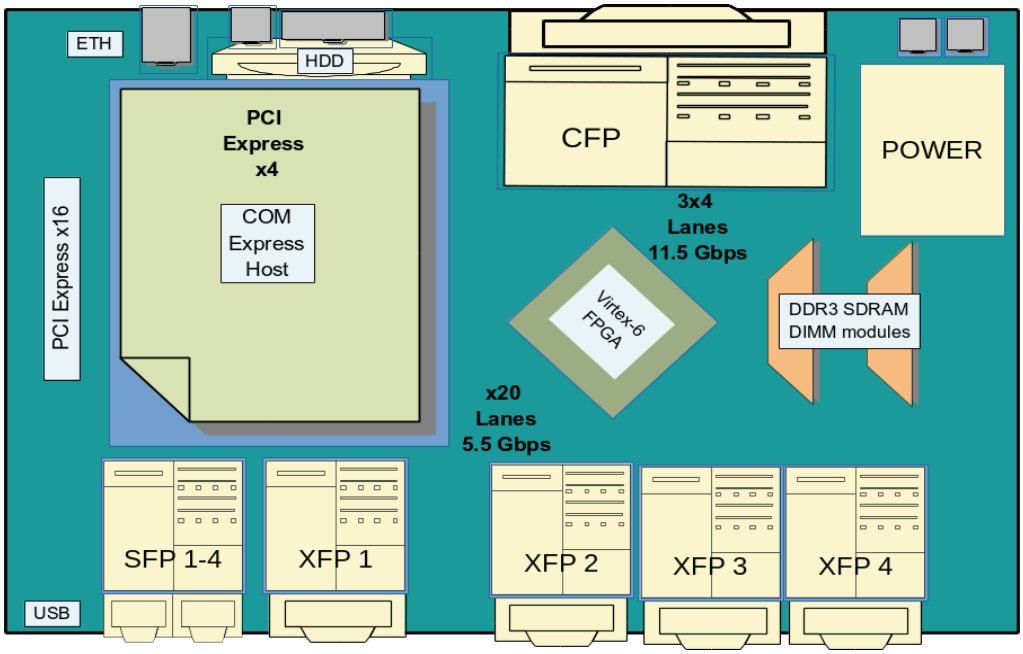
Popular C-GEP configurations

- CGEP_5X_1C:
  100 Gbit/s to 10 Gbit/s arbitrator - with 1x100 Gbit/s and 5x10 Gbit/s
- CGEP_5X_3Q:
  40 Gbit/s to 10 Gbit/s monitor board - with 3x40 Gbit/s and 5x10 Gbit/s
- CGEP_20G_4X:
  10 Gbit/s to 1 Gbit/s monitor board - with 4x10 Gbit/s and 20x1 Gbit/s



C-GEP comes with AITIA's own 100 Gbit/s FPGA IP core

- IEEE 802.3ba-2010 - a fully compliant implementation
  - Virtex 6 device specific GTH transceivers
  - Can be easily ported to other FPGAs
  - Rx/Tx MAC interface running at 312.5 MHz frequency, combined with 512 bits wide datapath
- Optimized Ethernet FCS calculation on Rx and Tx MAC interfaces
- Simple and configurable traffic generator application
- 100 Gbit/s throughput capable Protocol Parser (14-tuple) and Packet Filter
- Tested on C-GEP with CFP SR optical modules

Source code is available for further development!

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