C-GEP 20

Reference manual

Ver.: 20141107_v1.0

1. Introduction

1.1. What does CGEP-20 mean?

The CGEP-20 device is able to monitor two 10 Gbps links in real time and without packet loss, The received ethernet frames are first decoded, and filtered then stored in a temporaly DDR3 buffer, and finally streamed on a TCP connection. There are 19 1 Gb/s monitoring output interfaces in optical or copper SFP format. The data is received and processed by industrial monitoring PC-s on the other end. The monitoring software generates different statistics, call-detail-records (CDRs), or forward the incoming traffic to other receivers too.

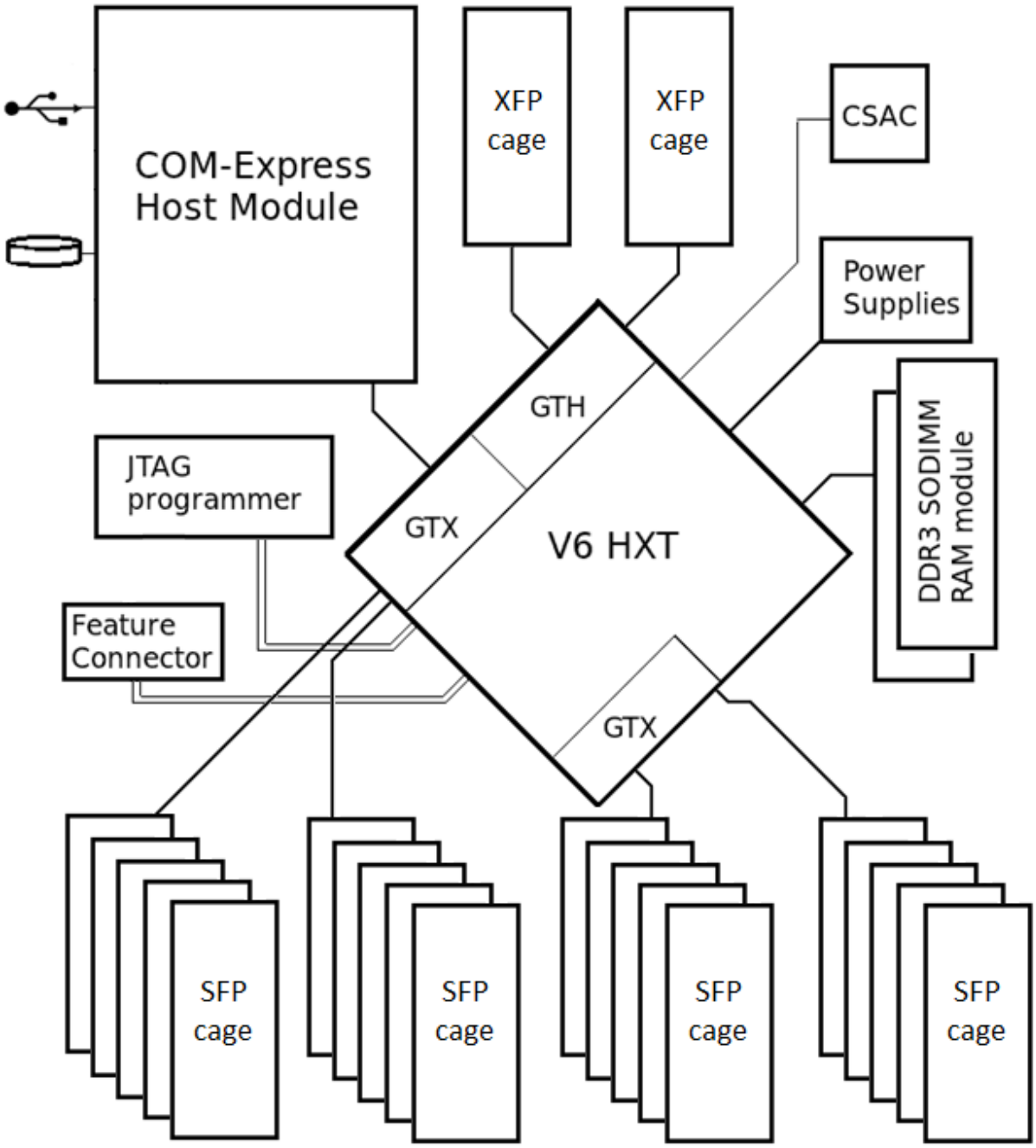
The monitored frames are timestamped with a high precision timestamp (64 bit, 8 ns resolution) upon reception. Because of the huge traffic load on 10 Gb/s links a high precision, and good resolution timestamp is very important. Also CDR assembly requires that packet arrivals must be distinguishable. C-GEP 20 guarantees that packets belonging to a transaction are always in sequence, and never swapped.

One of the key requirements is, that the C-GEP management user-interface has to be platform-independent the device must be easy to configure and to use. This means, that the user can access the device through an universal web-interface from any web browser.

1.2. What is on board of the C-GEP 20?

- Xilinx FPGA Chip (XC6VHX255T-2FFG1155C, or XC6VHX380T-1FFG1155C)
- 10 Gbit/s input interfaces
  - 2 XFP cages
- 1 Gb/s output interfaces
  - 19 SFP cages
  - The module may have copper or optical network interface
- 1 Gbit/s NTP time synchronization
  - 1 SFP cage
- DDR3
  - for temporaly monitoring data storage
  - 2 pcs, 512 MB/1 GB/2 GB capacity modules per socket (PC3-10600 SODIMM)
  - By default the device contains: MT8JSF25664HZ-1G4 (Micron Semiconductor)
- COREx: Microcontrollers for the 1/10 Gb/s interfaces
  - get interface statuses
  - controls interface functions (fe. Enable/disable transmission)
- Management Ethernet interface
  - 10/100/1000M interface connection to the onboard management PC
  - Allows access to the Web-UI
- VGA/PS2/USB/RS-232 connectors for external devices
  - Connects to the management PC
- HDD
  - For running the C-GEP Linux based-OS
  - Western Digital, 320 GB, 5200 rpm, notebook HDD
- Atomic clock
  - Optional
  - For high precision timestamping
  - Symmetricom SA.45s
- Built-in Xilinx-compatible JTAG programmer
  - FPGA firmware uploading
- Power supply
  - 400W, micro sized PC PSU

2. Architecture



2.1 Fig – Cages and modules connecting to the FPGA

The high speed interfaces (SFP, XFP, PCI-E) are directly connected to the FPGAs dedicated GTX/GTH transceivers.

2.1. The main properties of the FPGA chip onboard

	XC6VHX255T-2FF1155C	XC6VHX380T-1FF1155C
Slice array metric	170x240	214x360
Slices	39600	59760
LUT RAM	3050 kBytes	4570 kBytes
RAMB18 OR	1032x18KBytes	1536x18KBytes
RAMB36	516x36kBytes	768x36kBytes
DSP slices	576	864
GTX Transceivers	24	24
GTH Transceivers	12 (3 quad)	12 (3 quad)
Clock Management Tiles	12	18

Both chips contain:

- 2 PCI Express Endpoint controllers
- 2 Tri-mode (10/100/1000) Ethernet Media Access Controller (MAC) modules
- 2 Internal Configuration Access Ports (ICAP)

2.2. Interfaces, connectors

Front panel:

- 20 SFP transceiver cages
- Power LED (green)
- HDD LED (red)

Back panel:

- Power switch
- ATX power cord
- 1 USB connector
- Atomic clock PPS IN/OUT
- 2 XFP transceiver cage, with status LED-s
- 1 DSUB connector (VGA monitor)
- 1 RJ45 connector, 10/100/1000M Ethernet management LAN

Internal connectors:

- 2 DDR3 SODIMM SDRAM socket
- 1 COM (Computer On Module) Express connector

- 4 USB
- 2 SATA HDD connector to the COM Express Host
- Feature connectors for testing
- JTAG pin headers for testing

2.3. Management PC, Computer on Module

All C-GEP devices contain an x86 built in mini-PC for control and management. The mini-PC hosts a Linux base operating system (Ubuntu for now), which connects directly to the FPGA on a PCI-E x4 interface. The web-server is responsible for the graphical user interface for configuring and controlling the C-GEP 20 device. The mini-PC is connected to the network via 10/100/1000M Ethernet.

2.4. Clock sources

- 100 MHz
  - PCI-E reference clock
  - PCI-E v2.1 compliant external clock source
- 500 MHz
  - DDR3 reference clock
  - FXOLC735-500, 50PPM
- 300 MHz
  - Main clock source for the FPGA
  - FXOLC735-300, 50PPM
- 156.25 MHz
  - 1 common reference clock for XFP modules
  - CCPD033X-50-156.25, 50PPM
- 125 MHz
  - 2 reference clock source for the SFP modules (front and back panel SFP-s each require a clock source)
  - CCPD033-50-125, 50PPM

2.5. PCI Express x4

The FPGA chip communicates with the management PC-s OS through a dedicated PCI-E x4 interface.

2.6. DDR3 SODIMM RAM

The C-GEP platform supports 2 SODIMM socket DDR3 SDRAM modules.

By default we ship two PC3-10600 MT8JSF25664HZ-1G4, each module has 2 GB capacity.

2.7. Misc connectors

The C-GEP 20 device has 2 10 PIN connectors (J24, J26) inside the chassis for debug and testing purposes. These connectors can be used for SGA-ClockCard syncronization interface. The J24 and J26 connectors are directly connected to FPGA I/O pins.

Figure 2.7.1. shows the pinout according to the FPGA pin names.

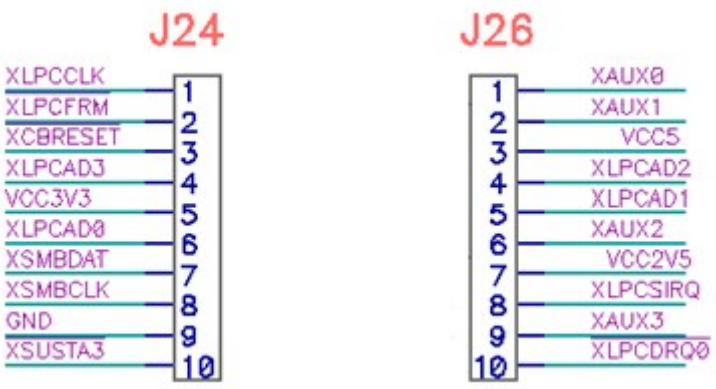


Fig. 2.7.1 – Pinout of the feature connector

2.8. Atomic clock

The platform supports a SA.45s type atomic clock module for high precision timestamping as an optional feature. The SMA type PPS in/outputs of the atomic clock are on the back of the C-GEP device. The SMA coaxial connectors have 75 ohm impedance match, and are voltage level matched, therefore they have a constant 10 ns delay.

Main properties:

- 10 MHz CMOS-compatible outputs

- 1 PPS output
- 1 PPS input for synchronization
- RS-232 interface
    - Control
    - Calibration
    - Internal time-of-day information readout

Note: The atomic clock has a 3 minutes warmup time to reach optimal working conditions.

Appendix

A.1. Pictures of the C-GEP 20 prototype (2x10 Gbit/s - 20x1 Gbit/s)

1. Fig. – Front view, C-GEP 20 prototype (without cover)

2. Fig. – Front view, C-GEP 20 prototype (with cover)

3. Fig. – Back view, C-GEP 20 prototype (without cover)