CGEP

Platform for high-speed networking

REFERENCE MANUAL

Ver.: v1_1

Contents

1. Introduction

1.1. What is CGEP?

CGEP is a Combination Gigabit (Ethernet) Evaluation Platform.

Wide range of applications can be deployed on this high speed platform - up to 100 Gbps:

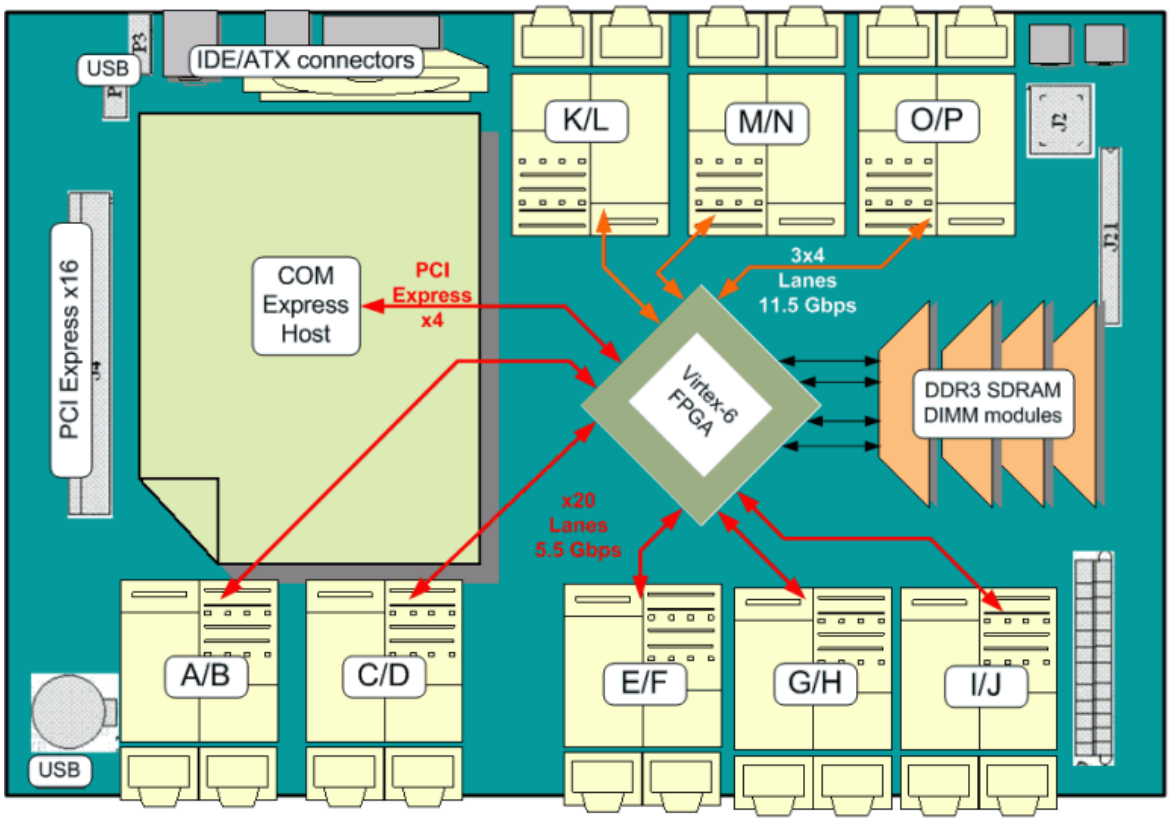
1. Monitoring – Traffic mix
    a. Traffic mix definition
    b. Measuring traffic mix, important attributes
2. Deep Packet Inspection
    a. Signature based application identification
    b. Statistical analysis by numerical properties
    c. Analysis by Behavior and Heuristics
    d. Chi-square classifier
3. IMS SIP Platform
4. Custom Switching/Routing
5. Video-Trans-Coding
6. Media Gateway
7. Firewall
8. Traffic Generator

Application features:

- 64 bit Timestamp with 4/8 nsec resolution,
- lossless packet capture limited only by host PC’s speed and resources,
- header-only capture: configurable protocol layer depth decoded by hardware on-the-fly,
- parameterized line speed capable packet/flow generator for active measurements,

1.2. What is on-board?

The figure below shows the major on-board components. (top view)



1.2.1. Architecture

CGEP occupies a standard 1U x 19 inch rack mount case, with active cooling on ATX style power supplies, and passive cooling on board.

Interface connectors are mounted on front, occupying slots A..J, since management, mains, and interface connectors K..P are on the rear panel.

The central part of the hardware is the Virtex 6 FPGA (XC6VHX255T-2FFG1155C, or XC6VHX380T-1FFG1155C).

The high speed interfaces (SFP, SFP+, XFP, QSFP, CFP, SATA and PCI-E slots) are connected to the FPGA's GTX or GTH transceiver ports. Several variation of interfaces are supported by the architecture - Gigabit Ethernet, 10/100 Ethernet, STM-16, 40 Gbps QSFP optic etc…

The actual facility depends on the product code as described in 1.4.

The applicable interface types with their identifiers:

```
G - SFP with Gigabit Ethernet support (copper/optical modules)
W - SFP with WAN support up to 2.5 Gbps incl. GPON OLT
A - SATA 2.0 on board connector to FPGA fabric
S - SFP+ with 10GE support
X - XFP supports 10GE
Q - QSFP for 40GE
C - CFP module receptacle for 100GE
```

There are a good number of ways to assign them to the designated board positions A/B, C/D, E/F, etc...

There is a Type-2 COM Express module receptacle mounted on-board. This feature allows a computer on module to be used for control and management. It is connected to the fabric by a high speed PCI Express x4 link.

Typical ATX connectors are mounted on the rear panel, including several USB-A receptacle, management LAN, VGA, PS/2 keyboard and mouse.

Two DDR3 SDRAM DIMM module can be installed to form a 128 bits wide data path to their gigabytes capacity.

1.2.2. Interfaces and connectors

Front mounts:

- 1 USB host connector
- Power and HDD LED
- 5 positions for various high-speed network interface quads with status LEDs utilizing GTX transceivers

Rear mounts:

- 1 Power button and Mains connector
- 1 PS/2 Keyboard
- 1 PS/2 Mouse
- 3 positions for various high-speed networking interface quads with status LEDs utilizing GTH transceivers
- 1 DSUB connector for VGA monitor
- 1 USB host connector (+1 internal for booting a pendrive, and 4 more on pin headers)
- 1 RJ45, 10/100 Ethernet for management LAN

Internal mounts:

- 2 DDR3 SODIMM SDRAMs
- 1 COM (Computer On Module) Express receptacle
- 4 USB
- 2 SATA HDD connectors for COM Express host
- xSATA 3.x HDD connectors for the FPGA – depending on the product code

1.2.3. Computer On Module

The management computer of the CGEP is implemented using a COM Express Type-2 (or higher) child board, running Linux or Windows operating system.

1.3. Conformity

CGEP aims the following Standards/Recommendations for its different type of interfaces designated:

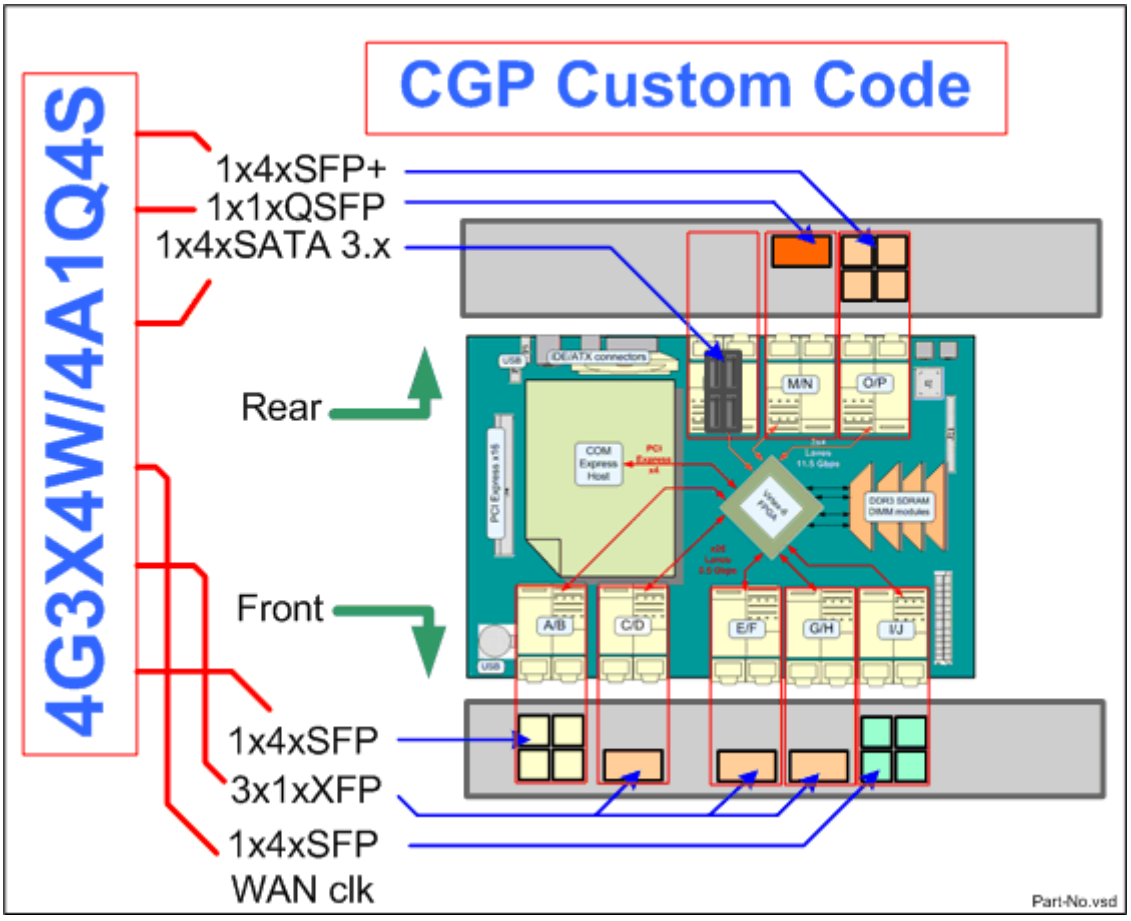
	SFP_	Small Formfactor Pluggable Transceivers
		SFF Committee INF-8074i Specification for SFP Transceiver
		SFF Committee SFF-8075 Specification for PCI Card Version of SFP Cage
		SFF Committee SFF-8472 Specification for Diagnostic Monitoring Interface for Optical Xcvrs
W	**_SDH**	Synchronous Digital Hierarchy
		ITU-T G.707/Y.1322 Network node interface for the synchronous digital hierarchy (SDH)
G	**_GBE**	Gigabit Ethernet (Optical/Copper)
		IEEE Std 802.3 Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications,SECTION THREE

X	**XFP_**	10 Gigabit Small Form Factor Pluggable Module
		SFF Committee INF-8077i 10 Gigabit Small Form Factor Pluggable Module
S	**SFP+_**	Enhanced Small Formfactor Pluggable Transceivers
		SFF Committee SFF-8431 Specifications for Enhanced Small Form Factor Pluggable Module SFP+
	_10GE	Ten Gigabit Ethernet (Optical/Copper) IEEE Std 802.3 Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications,SECTION FOUR
Q	**QSFP_**	QSFP+ 10 Gbps 4X PLUGGABLE TRANSCEIVER
		SFF Committee SFF-8436 Specification
	_40GE	40 Gbps Ethernet (Optical)
C	**CFP_**	C Form-factor Pluggable
		CFP MSA Hardware Specification Revision 1.4
	_100GE	100 Gbps Ethernet (Optical)
		IEEE Std 802.3ba Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications, Amendment 4: Media Access Control Parameters, Physical Layer, and Management Parameters for 40 Gb/s and 100 Gb/s Operation
A	**SATA**	Serial Advanced Technology Attachment
		Serial ATA International Organization: Serial ATA Revision 3.0
	PCIE	**PCI Express**
		PCI-SIG PCI Express Base Specification Revision 1.0a
		PCI-SIG PCI Express Card Electromechanical Specification Revision 1.0a

	DDR3	**Dual Data-Rate III. SDRAM and Modules**
		JEDEC JESD79-3E DDR3 SDRAM STANDARD

1.4. Product Codes

Product codes consist of number+letter combinations in the following format: **CGP-nnZ[mmY]../jjM[kkL]..**
where *nn*, and *mm* are the numbers of *Z* and *Y* type interfaces on the front panel, since *jj*, and *kk* are the numbers of *M* and *L* type interfaces on the rear panel as shown below.



The letter codes for the different interface types:

```
G - SFP with Gigabit Ethernet support (copper/optical modules)
W - SFP with WAN support up to 2.5 Gbps incl. GPON OLT
A - SATA 2.0 on board connector to FPGA fabric
S - SFP+ with 10GE support
```

```
X - XFP supports 10GE
Q - QSFP for 40GE
C - CFP module receptacle for 100GE
```

Front capacity is 5x4x5Gbps (100Gbps total) (20x6.6 Gbps max.) For the five slots on the front, type **G**, **A**, **S**, and **X** interfaces can be selected plus one W on the rightmost position, resulting

```
(4 on 5)*(4 on 4) =
((4+5-1)!/((4-1)!*5!))*((4+4-1)!/((4-1)!*4!))=
56*35 = 1960 configurations.
```

Rear capacity is 3x4x10Gbps (120Gbps total).
For three GTH quads on the rear, type **A**, **S**, **X**, and **Q** interfaces can be selected, plus one unique **C** consuming all slots, resulting

```
(4 on 3)+1 =
((4+3-1)!/((4-1)!*3!))+1 = 21 configurations.
```

Therefore the overall CGEP product range consists of **41160** different interface combinations.

For examples, a **CGP-20G/3Q** has 20 Gigabit Ethernet capable SFPs on the front and 3 pieces of 40GE QFPs on the rear.

Here is the table for the developer's version of CGEP:

Product code	**Front IF quad**					**Rear quads**			**Brand**
	A B	C D	E F	G H	I J	K L	M N	O P	
4A1X1S4G4W/4A4S1Q	A	X	S	G	W	A	S	Q	40G Test board (XLGT)
4A1X1S4G4W/1C	A	X	S	G	W	C	C	C	100G Test board (CGT)

Typical brands for frequently used applications:

Product code	Front IF quad					Rear quads			Brand
	A B	C D	E F	G H	I J	K L	M N	O P	
4A4S/4S2Q	A	S	S	S	S	S	Q	Q	40G Monitor SFP+ drop and trace to disk (XLMSTD)
5S/4S2Q	S	S	S	S	S	S	Q	Q	40G Monitor SFP+ drop (XLMS)
4A4X/4X2Q	A	X	X	X	X	X	Q	Q	40G Monitor XFP drop and trace to disk (XLMXTD)
5X/4X2Q	X	X	X	X	X	X	Q	Q	40G Monitor XFP drop (XLMX)
20G/1C	G	G	G	G	G	C	C	C	100G Monitor SFP* drop (CMG)
20G/12A	G	G	G	G	G	A	A	A	GE Grabber (GEG)
20A/1C	A	A	A	A	A	C	C	C	100Grabber (CGR)
20A/4A2Q	A	A	A	A	A	A	Q	Q	40Grabber (XLGR)

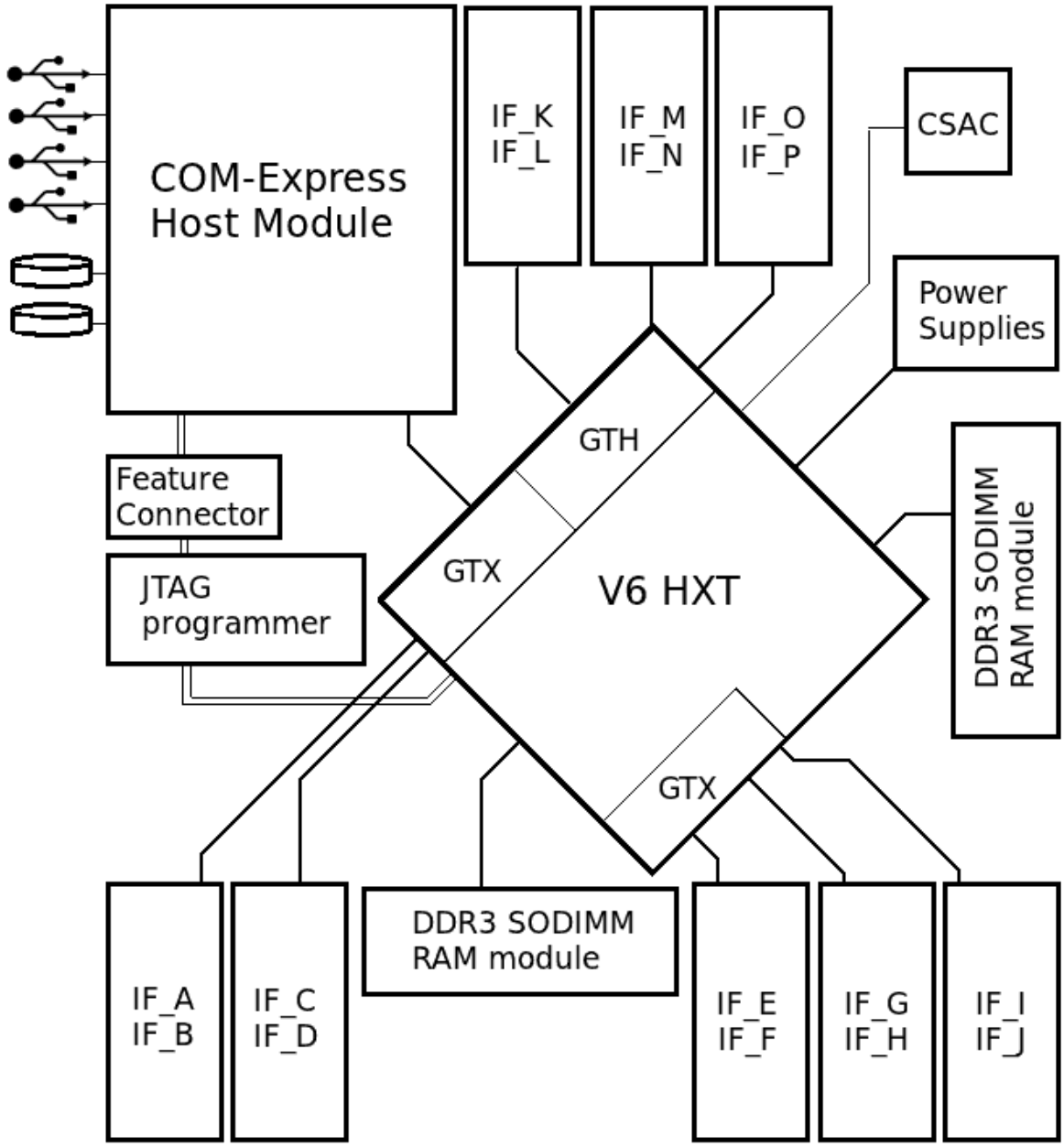
Product code	Front IF quad					Rear quads		
	A B	C D	E F	G H	I J	K L	M N	O P
20G/12S	G	G	G	G	G	S	S	S
20G/8S4X	G	G	G	G	G	S	S	X
20G/8S1Q	G	G	G	G	G	S	S	Q

20G/4S8X	G	G	G	G	G	S	X	X
20G/4S4X1Q	G	G	G	G	G	S	X	Q
20G/4S2Q	G	G	G	G	G	S	Q	Q
20G/4X2Q	G	G	G	G	G	X	Q	Q
20G/3Q	G	G	G	G	G	Q	Q	Q
20G/4A8S	G	G	G	G	G	A	S	S
20G/4A4S4X	G	G	G	G	G	A	S	X
20G/4A4S1Q	G	G	G	G	G	A	S	Q
20G/4A8X	G	G	G	G	G	A	X	X
20G/4A4X1Q	G	G	G	G	G	A	X	Q
20G/4A2Q	G	G	G	G	G	A	Q	Q
20G/1C	G	G	G	G	G	C	C	C
5S/12S	S	S	S	S	S	S	S	S
. . . . .	...	...	...	...	...	...	...	...
5S/4A4X1Q	S	S	S	S	S	A	X	Q
5S/4A2Q	S	S	S	S	S	A	Q	Q
5S/1C	S	S	S	S	S	C	C	C
5X/12S	X	X	X	X	X	S	S	S
5X/8S4X	X	X	X	X	X	S	S	X
. . . . .	...	...	...	...	...	...	...	...

5X/4A4X1Q	X	X	X	X	X	A	X	Q
5X/4A2Q	X	X	X	X	X	A	Q	Q
5X/1C	X	X	X	X	X	C	C	C
12G2X/12S	G	X	X	G	G	S	S	S
12G2X/8S4X	G	X	X	G	G	S	S	X
12G2X/8S1Q	G	X	X	G	G	S	S	Q
12G2X/4S8X	G	X	X	G	G	S	X	X
. . . . .	...	...	...	...	...	...	...	...
12G2X/4A4X1Q	G	X	X	G	G	A	X	Q
12G2X/4A2Q	G	X	X	G	G	A	Q	Q
12G2X/1C	G	X	X	G	G	C	C	C
4A16G/12S	A	G	G	G	G	S	S	S
4A16G/8S4X	A	G	G	G	G	S	S	X
. . . . .	...	...	...	...	...	...	...	...
. . . . .	...	...	...	...	...	...	...	...

2. Architecture

The simple and robust architecture of CGEP is shown on the block diagram below.



The heart of the board is a Xilinx Virtex-6 family FPGA device.

The PCB can accomodate two types of devices:

- XC6VHX255T-2FFG1155C (for CGP board)
- XC6VHX380T-1FF1155C (for CGPX board)

The main characteristics of the devices are shown in the table below:

	XC6VHX255T-2FF1155C	XC6VHX380T-1FF1155C
Slice array metric	170x240	214x360
Slices	39600	59760
LUT RAM	3050 kBytes	4570 kBytes
RAMB18 OR	1032x18KBytes	1536x18KBytes
RAMB36	516x36kBytes	768x36kBytes
DSP slices	576	864
GTX Transceivers	24	24
GTH Transceivers	12 (3 quad)	12 (3 quad)
Clock Management Tiles	12	18

In addition, both types have:

- Two PCI Express Endpoint Controller
- 2 Tri-mode (10/100/1000) Ethernet Media Access Controller (MAC)
- 2 Internal Configuration Access Ports (ICAP)

The following sections detail the rest of the board's architectural elements.

2.1. Data rates and reference clocks

There are several clock sources available on CGEP for the FPGA cores various interface standards. The following table shows their names, nominal frequencies, designated FPGA pins, and their application.

Signal	f [MHz]	FPGA#	Application
PERCKN	100.00	AA7	PCI Express Hosts reference
PERCKP	-	AA8	.
CK533N	500.00	V27	DDR3 reference clock
CK533P	(XO)	V26	.
CK300N	300.00	V27	Main system clock
CK300P	(XO)	V26	.
RCKKLP *	156.25	P6	XFP (XFI)
RCKKLN	(XO)	P5	K/L
RCKMNP *	156.25	H2	XFP (XAUI)
RCKMNN	(XO)	H1	M/N
RCKOPP *	156.25	C4	XFP (XAUI)
RCKOPN	(XO)	C3	O/P
RCKABP0 *	125.00	AG8	SFP Tri-Mode Ethernet App.
RCKABN0	(XO)	AG7	10/100/1000 Mbps
RCKGHP0 *	125.00	AG27	SFP Tri-Mode Ethernet App.
RCKGHN0	(XO)	AG28	10/100/1000 Mbps

* These clock references are routed to dedicated GT clock pins.
XO designates LVPECL Crystal Oscillators.

2.2. Multi gigabit interfaces

Depending on the actual product code, CGEP supports a wide variety of multi gigabit networking interfaces as well as SATA3 storage devices.

Front interfaces utilizes Xilinx Virtex-6 GTX transceiver lanes, 5.5 Gbps each, since aft section uses GTH transceiver quads for 10, 40 or 100 Gbps applications.

CGEP can also supports SATA 3.0 interfaces for high speed mass storage devices. SATA connectors occupies internal mounts.

Section 3. describes these interfaces in depth, and refer 1.4 to evaluate the actual set of interfaces according to the product code.

There are separate interface control signals for front and aft interfaces. Both normal and Low Voltage MDIO signals are available as well as the proprietary mcmd/mres serial communication lines.

Signal	**Pos.**	**FPGA#.**	**Signal**	**Pos.**	**FPGA#**
MCMDA	Front	N34	MRESA	Front	M34
MDIOA	.	P34	MDCLKA	.	T34
LVMDIOA.		AN26	LVMCKA	.	AP24
MCMDK	Aft	A14	MRESK	Aft.	A13
MDIOK	.	A12	MCLKK	.	A10
LVMDIOK.		K23	LVMCKK	.	J23

2.3. PCI Express x4 Endpoint

The PCI Express endpoint allows an FPGA design to support x1, and x4 gigabit lanes to communicate with the host module, at the speed of 2.5 Gbps of each.

The table below lists the connectors pins and any associated FPGA connectivity.

Signal	FPGA#	Signal	FPGA#
PERCKP	AA8		
PERCKN	AA7		
PERP0	AB1	PETP0 *	AC4
PERN0	AB2	PETN0 *	AC3
PERP1 **	W3	PETP1 *	Y6
PERN1 **	w4	PETN1 *	Y5
PERP2	Y1	PETP2 *	AB6
PERN2	Y2	PETN2 *	AB5
PERP3	V1	PETP3 *	AA4
PERN3	V2	PETN3 *	AA3

* RXPOLARITY attribute of the GTX has to be changed

** TXPOLARITY attribute of the GTX has to be changed

Although the PCI identification codes are FPGA core dependeant, defaults are the following:

```
Vendor ID........ 15C6 ..... Technical University of Budapest
Device ID........ C6EB ..... CGEP board
Revision ID......    1 ..... Rev. 1. (CGEP)
Base Class.......   02 ..... Network controller
Sub-Class........   80 ..... Other network controller
Interface........    0 ..... Base model, XC6VHX255T
Interface........    1 ..... Deluxe, XC6VHX380T
```

2.4. DDR3 SODIMM RAM

The CGEP board contains two 204-pins small-outline dual in-line memory module (SODIMM) receptacle (J1,J2) that supports installation of DDR3 SDRAM SODIMMs.

A 2Gbytes capacity PC3-10600 SODIMM (Micron Semiconductor) part number MT8JSF25664HZ-1G4 is shipped with CGEP - by default.

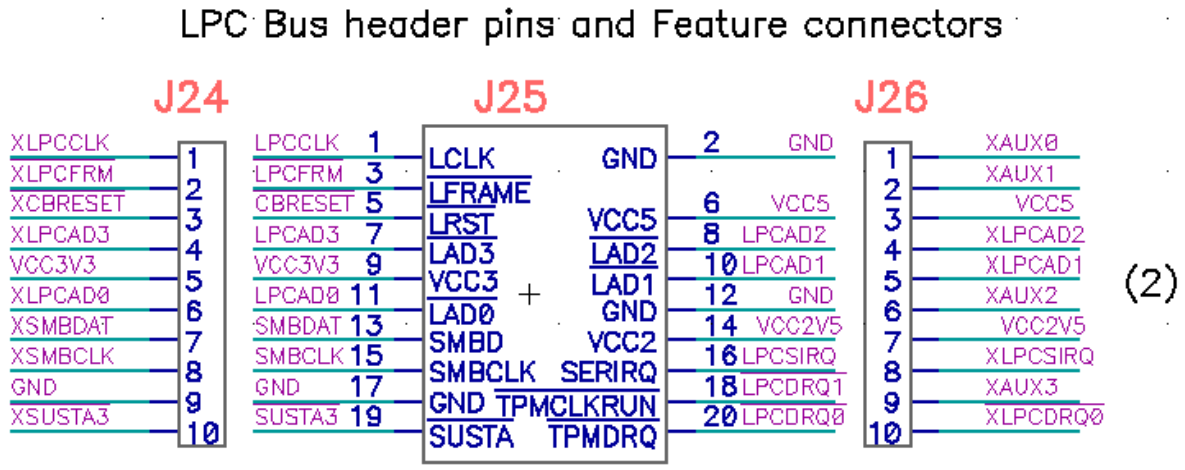
The SODIMM interface may support customer installation of DDR3 SODIMMs too.

2.5. Feature Connector

CGEP has 4x10 pins Feature Connector (designated as J24, J25, J26).

The center pin header is compatible with the Low Pin Count Bus (LPC), and routed to the COM express host module. Side headers are connecxted to the FPGA.

The figure and the table below shows the pinout of the LPC connector and the corresponding FPGA pins.



Signal	J24#	FPGA#.	Signal	J25#	FPGA#
XLPCCLK	01	H13	XAUX0	01	K11
~XLPCFRM	02	K13	XAUX1	02	K12
~XCBRESRT	03	J13	VCC5	03	---
XLPCAD3	04	G12	XLPCAD2	04	L10
VCC3V3	05	---	XLPCAD1	05	L12
XLPCAD0	06	H12	XAUX2	06	M10
XSMBDAT	07	H11	VCC2V5	07	---
XSMBCLK	08	L13	XLCPSIRQ	08	M12
GND	09	---	XAUX3	09	N11
~XSUSTA3	10	J11	~XLPCDRQ0	10	M11

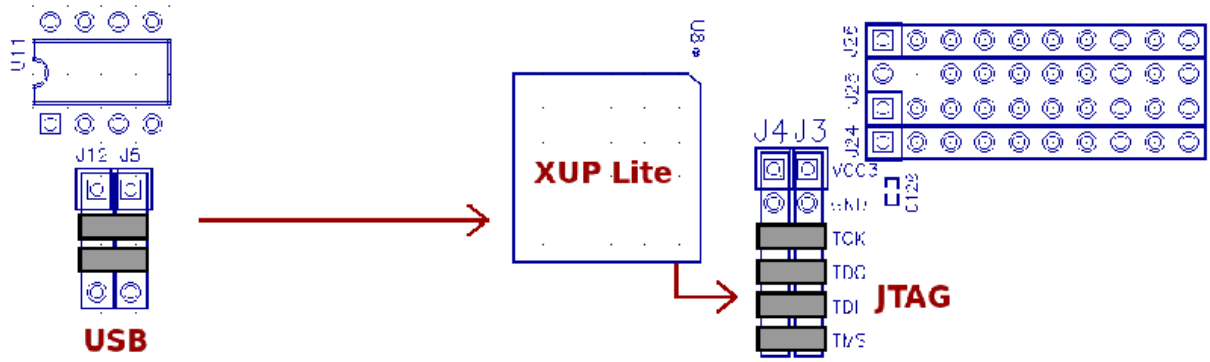
Warning! **The LPC bus signalling based on 3.3V logic, since the FPGA I/O-s powered from 2.5V. Direct connection is not possible, use level shifters.**

2.6. FPGA Programming

Two configuration methods are supported by CGEP to upload (program) the FPGA core.

2.6.1. Built in JTAG programmer

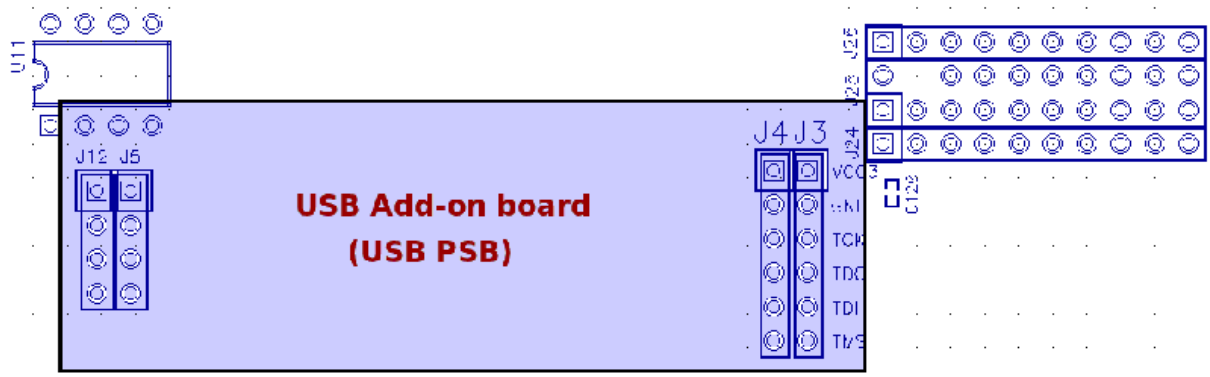
FPGA core can be loaded directly through the JTAG port (designated as J3) using the built-in programmer. In order to use the built in programmer, a set of jumpers have to be installed as shown in the figure below.



XUP-Lite is compatible with the platform USB II cable.

2.6.2. USB Programming Solution Board

Standalone or USB driven programming soulution is possible using an add-on card as shown below:



Typical PSB (Programming Solution Board) contains an SD card reader, and a microcontroller. If there is no host board installed, only a standalone solution can be used to program the FPGA.

2.7. Status LEDs

In addition to the status lights of the network interfaces, the following LEDs are available on-board for diagnostic purpose:

Signal	LED	Position	FPGA#
C0INIT	Green	D11	N33
C0ERR	Red	D3	R28
C1INIT	Green	D12	P30
C1ERR	Red	D4	N27

2.8. Chip Scale Atomic Clock

CGEP has a Symmetricom SA.45s type atomic clock on-board. The control and timing signals are summarized below:

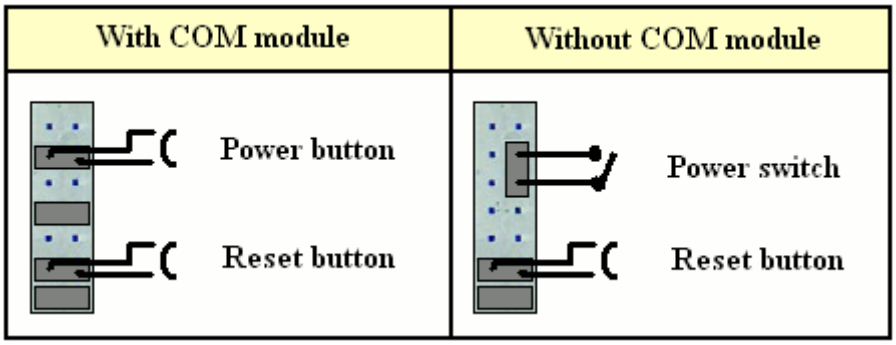
Signal	Pos.	FPGA#	.Signal	Pos.	FPGA#
XPPSI	P5	D10	XPPSO	P6	C13
APPSI	U25/9	C11	APPS	U25/10	C12
ATX	U25/5	B11	ARX	U25/6	D11
ALOCK\	U25/4	B10	AQ10	U25/12	B12
ATUNE	U25/1	D13			

External PPS signals (P5 in, and P6 out) carried over 75 ohms coaxial cables/connectors (SMA). Nominal levels at the termination is 1.5 Vpp. Note that level shifters are inserted between the chip and the FPGA - itroducing cca. 10 nsec delay on each signals. Also note that it takes two minutes or so to warm up the atomic clock physics.

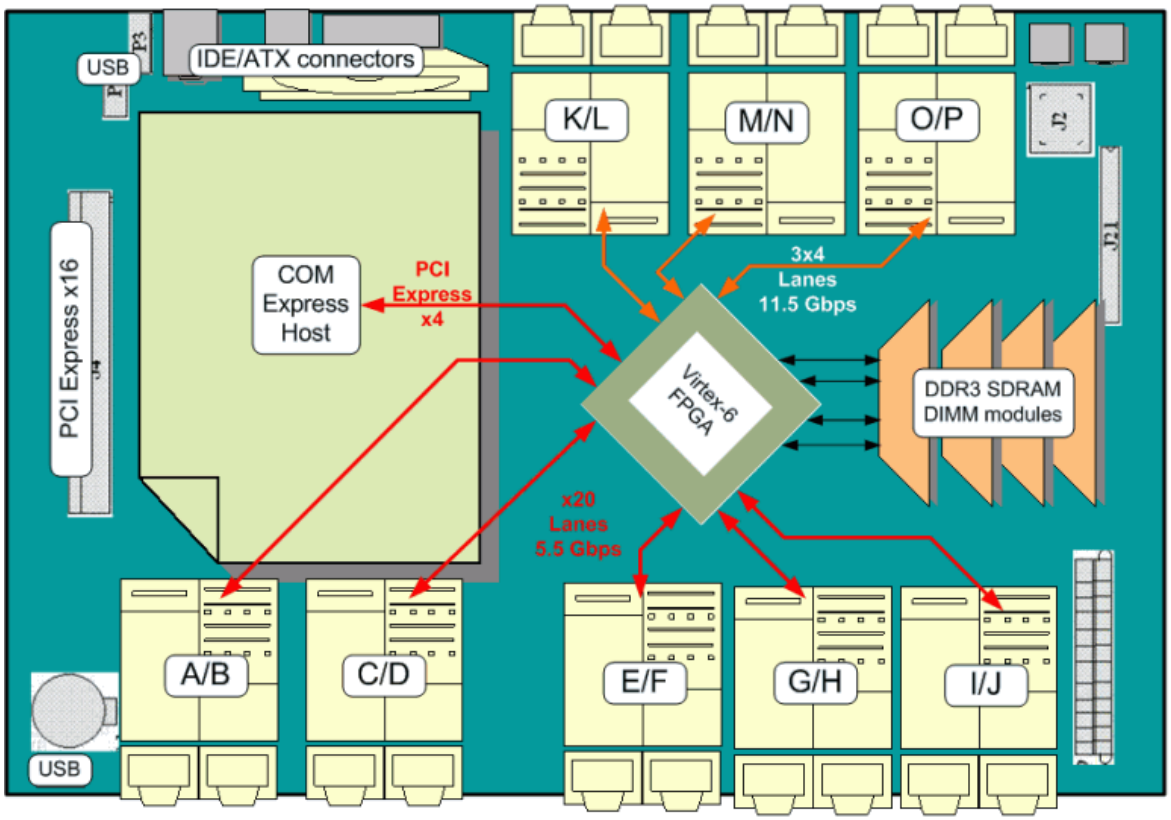
2.9. COM Express host

CGEP can accomodate a Type2 COM (Computer On Module) Express addon card. It is connected to the FPGA core with 4 lanes PCI Express link. Optionally, the LPC bus can also be connected to the feature connector using external level shifters.

Using a COM Express host is optional. If not installed, the power-up control has to be changed on J15..23 jumper block as shown in the figure below. A standalone PSB has to be used for FPGA programming in this case.



3. Interfaces



3.1. Front mounted dual SFPs Tri-Mode Ethernet

The CGEP board can be configured using dual SFP cages supporting 10/100/1000Mbps Tri-Mode Ethernet operations using the appropriate optical or copper modules.

Supported positions are A, B, C, D, E, F, G, H, I, and J. Aft section's GTH transceivers does not support ths type of interface.

An dual SFP on front consumes two lanes of GTX transceivers. That is half of five front quads, depending on the product code.

Dedicated 125.00 MHz reference clock source is available for FPGA reference.

The CGEP board provides filtered 3.3V power to dual SFP modules as per the SFP MSA.

3.2. Front mounted XFPs/SFP+ for 10Gbps Ethernet

The CGEP boards front side can accomodate upto 5 XFP/SFP+ cages supporting 10 Gigabit Ethernet (10Gbps) modules.

10G is implemented with an external XAUI-XFI converter chip (TI).

An XFP/SFP+ on front consumes four lanes of GTX transceivers: (A..B), (C..D), (E..F), (G..H), (I..J).

Dedicated 156.25 MHz reference clock source is available for FPGA reference.

3.3. Front mounted SFP+ implementing Fibre Channel

The CGEP board can be configured using dual SFP+ cages supporting Fibre Channel x1 – x4 operations using the appropriate optical modules.

Supported positions are A, B, C, D, E, F, G, H, I, and J. Aft section's GTH transceivers does not support ths type of interface.

A dual SFP+ on front consumes two lanes of GTX transceivers. That is half of five front quads, depending on the product code.

Dedicated 212.5 MHz reference clock source is available for FPGA reference.

The CGEP board provides filtered 3.3V power to dual SFP+ modules as per the SFP+ MSA.

3.4. Rear mounted XFPs/SFP+ for 10Gbps Ethernet

The CGEP board can be configured using rear XFP/SFP+ cages supporting 10 Gigabit Ethernet (10Gbps) modules.

Supported positions are K, L, M, N, O, and P. Aft section features direct XFI interfacing to the XFP/SFP+ modules, therefore XFI/XAUI conversion is not needed - although the possibility has T.B.D.

An XFP/SFP+ on rear consumes two lanes of GTH transceivers. One for transmitting reference to the XFP/SFP+, and one for data TRX. That is half of one of the rear quads (depending on the product code).

Dedicated 156.25 MHz reference clock source is available for FPGA reference.

3.5. Rear mounted CFP for 100Gbps Ethernet

The CGEP board can be configured using rear CFP cage supporting 100 Gigabit Ethernet (100Gbps) module.

A CFP on front consumes three GTH-quad transceivers, and twelve GTH lanes. One lane for transmitting reference to the CFP, and ten lanes for data TRX.

That is all of the rear GTH quads available for interfaces.

Three dedicated 156.25 MHz reference clock sources are available for FPGA reference.

3.6. Rear mounted CFP for 3x40Gbps Ethernet

The CGEP board can be configured using rear QFP cages supporting 40 Gigabit Ethernet (40Gbps) modules.

A QFP on front consumes one GTH-quad transceiver, and four GTH lanes.

Three dedicated 156.25 MHz reference clock sources are available for FPGA reference.

4. CORREs Interface controllers

4.1. Overview

COREx is a 44-Pin High-Performance dual SFP line interface module controller based on PIC18F45J10 from Microchip.

Multiple blocks of module receptacles available on CGEP designated as PA1, PB1, ... PJ1. Each block has its own COREx controller loaded with individual firmware designated as COREA, COREG, ... COREX, and commenced from the FPGA fabric using serial communication lines.

For example a dual SFP+ receptacles uses CORES type controllers, since XFP modules use COREX.

4.2. Module control commands and status

There are two major types of communication implemented in COREx, unicast, and broadast.

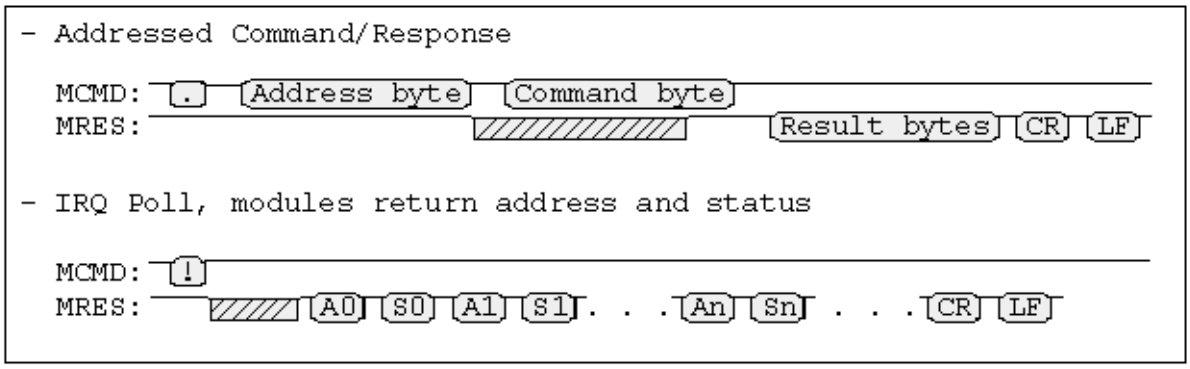
In case of unicast communication MHC sends 0x2E (period), followed by the address of the designated module. Interface 0 is addressed by 0x30 (ASCII zero character), 1 is 0x31, etc. . .

The next byte can be a command, or a query as shown below. Controllers do not echo back the MCMD characters, just interpret them.

Once a controller is addressed and start executing the command/query, all others release the MRES bus, and start snooping the activity on it upon the active unit returns results. Once idle state detected, all units become online again.

Broadcast is used to bring all units up at once, and request IRQ status, etc...

The next figure shows the timing of the command/response protocol.



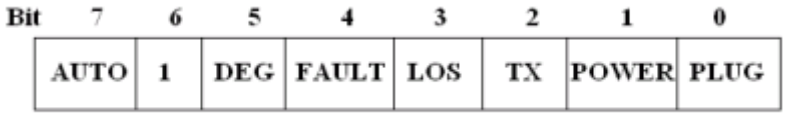
The command set and descriptions are summarized below:

Mnemonic	Code	ASCII	Description
MOD_RST	0x7E	~	Reset
MOD_AON	0x41	A	Activity LED On
MOD_FON	0x46	F	Fault LED On
MQRY_LONG	0x49	I	Module Details
MOD_AOFF	0x61	a	Activity LED Off
MOD_DEG	0x64	d	Degraded rate
MOD_FOFF	0x66	f	Fault LED Off
MQRY_IDN	0x69	i	Module ID
MOD_LON	0x6C	l	Laser on
MQRY_MAC	0x6D	m	Returns MAC address
MOD_NOR	0x6E	n	Normal rate

MOD_LOFF	0x6F	o	Laser off
MOD_PON	0x70	p	Power on
MOD_POFF	0x71	q	Power off
MQRY_STA	0x73	s	Returns Module Status
MOD_HOST	0x74	t	Takeover (host)
MOD_AUTO	0x75	u	Automatic up
MQRY_VER	0x76	v	Returns FW version
MOD_DOWN	0x78	x	Takeover and down

Note:
s,**u**,**x** and **~** commands can also be broadcasted

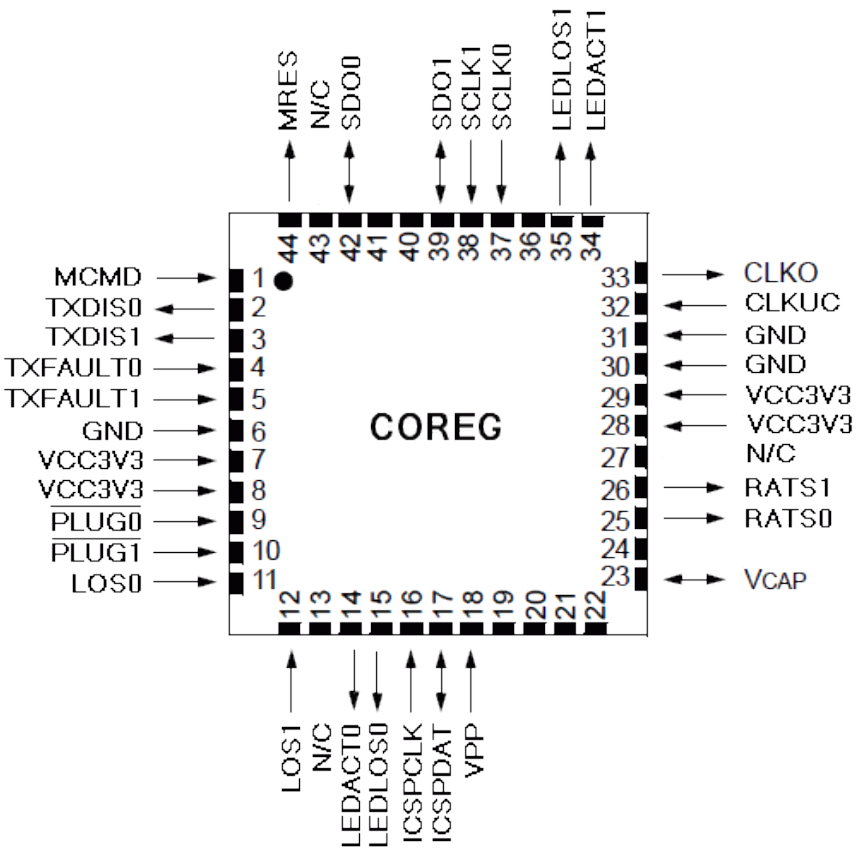
The status bits arrangement, and the corresponding defineants:



Mnemonic	Code	ASCII	Description
MSTA_EMPTY	0x40	@	Empty
MSTA_DOWN	0x41	A	Administrative down
MSTA_TESTING	0x43	C	Admin testing
MSTA_UP	0x47	G	Admin up and Go

MSTA_UP_FAULT	0x57	W	Up but faulted
MSTA_UP_DEGRADED	0x67	g	Admin up degraded
MSTA_UP_DEGFAULT	0x77	w	Degraded, Faulted
MSTA_LOS	0x4F	O	LOS alarm but up
MSTA_UP_LOSF	0x5F	_	LOS+Fault
MSTA_UP_LOSD	0x6F	o	LOS+RATS
MSTA_UP_LOSFD	0x7F	[DEL]	. . . bricked

4.3. COREG pinout and description

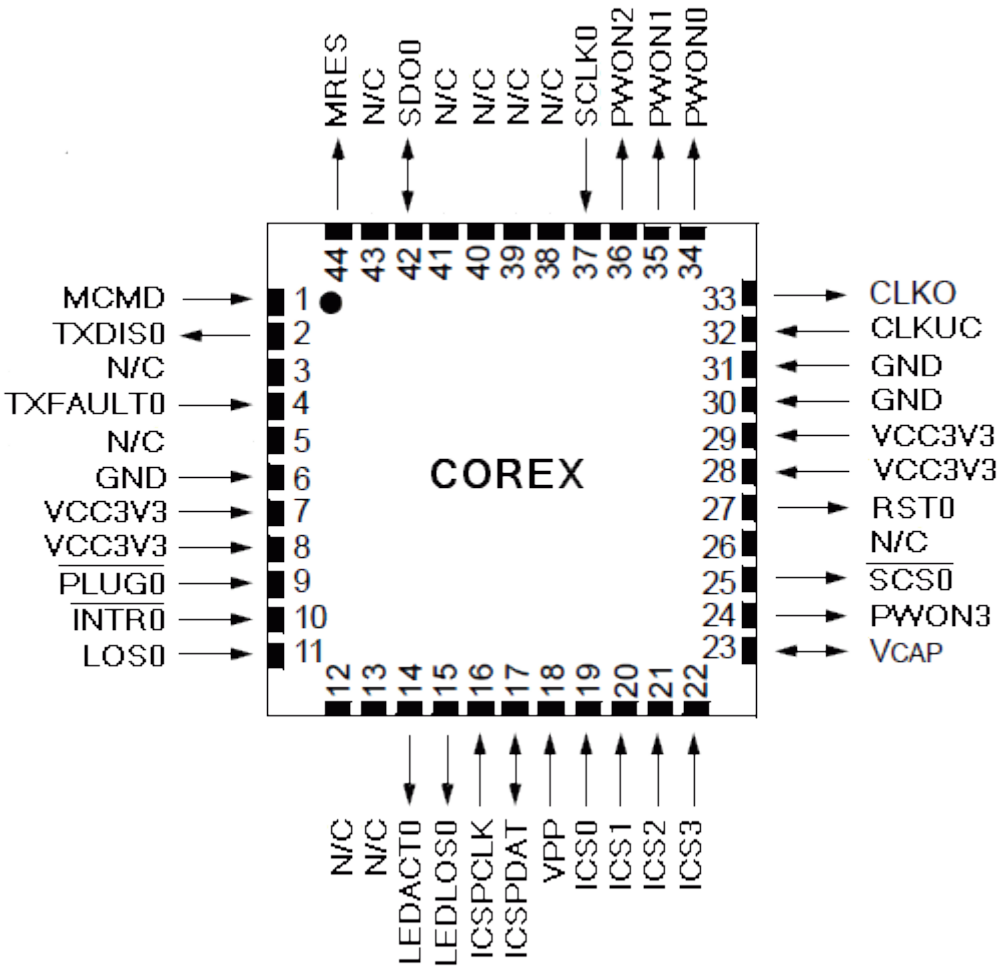


Pin name	Pin number	Type	Description
CLKUC	32	Input	24 MHz clock input
CLKO	33	Output	Clock output
MCMD	1	Input	Module command from MHC (115200,8,N,1)
MRES	44	Tristate	Module response
ICSPCLK	16	Input	In system programming clock
ICSPDAT	17	In/Out	In system programming data

VPP	18	Power	In system programming voltage
GND	6,30,31	Power	Power return (ground)
VCC3V3	7,8,28,29	Power	Power voltage, 3.3V nominal
SFP 0 (lower cage) signals			
LEDACT0	14	Output	Activity LED output (green)
LEDLOS0	15	Output	Alarm LED output (red)
TXDIS0	2	Output	Disable transmission (laser off)
TXFAULT0	4	Input	Transmitter fault condition
PLUG0	9	Input bar	SFP module present (low)
LOS0	11	Input	Loss Of Signal alarm
RATS0	25	Output	Full bandwidth
SCLK0	37	Output	IIC clock (module definition)
SDO0	42	In/Out	IIC data (module definition)
SFP 1 (upper cage) signals			
LEDACT1	34	Output	Activity LED output (green)
LEDLOS1	35	Output	Alarm LED output (red)
TXDIS1	3	Output	Disable transmission (laser off)

TXFAULT1	5	Input	Transmitter fault condition
PLUG1	10	Input bar	SFP module present (low)
LOS1	12	Input	Loss Of Signal alarm
RATS1	26	Output	Full bandwidth
SCLK1	38	Output	IIC clock (module definition)
SDO1	39	In/Out	IIC data (module definition)

4.4. COREX



Pin name	Pin number	Type	Description
CLKUC	32	Input	24 MHz clock input
CLKO	33	Output	Clock output
MCMD	1	Input	Module command from MHC (115200,8,N,1)
MRES	44	Tristate	Module response
ICSPCLK	16	Input	In system programming clock

ICSPDAT	17	In/Out	In system programming data
VPP	18	Power	In system programming voltage
GND	6,30,31	Power	Power return (ground)
VCC3V3	7,8,28,29	Power	Power voltage, 3.3V nominal
XFP signals			
LEDACT0	14	Output	Activity LED output (green)
LEDLOS0	15	Output	Alarm LED output (red)
TXDIS0	2	Output	Disable transmission (laser off)
TXFAULT0	4	Input	Transmitter fault condition
PLUG0	9	Input bar	XFP module present (low)
LOS0	11	Input	Loss Of Signal alarm
SCS0	25	Output bar	Chip select
SCLK0	37	Output	IIC clock (module definition)
SDO0	42	In/Out	IIC data (module definition)
INTR0	10	Input bar	XFP interrupt
RST0	27	Output	XFP reset/power down

5. Software Architecture

The CGEP-boards are preinstalled with a Linux-based operating system. The operating system is running on the COM-express host module (see: 2.9)

The host operating system is responsible for the following functions:

- loading, and reloading the FPGA firmware as needed
- resetting, and initializing the application-core
- hosting a web-interface for managing the device
- configuring and maintaining the board, polling statistics, and measurement results

5.1. Firmware loading

The default firmware is stored on the hard-disk, and is loaded automatically upon booting.

It is also possible to upgrade the firmware on-the-fly via the web-interface.

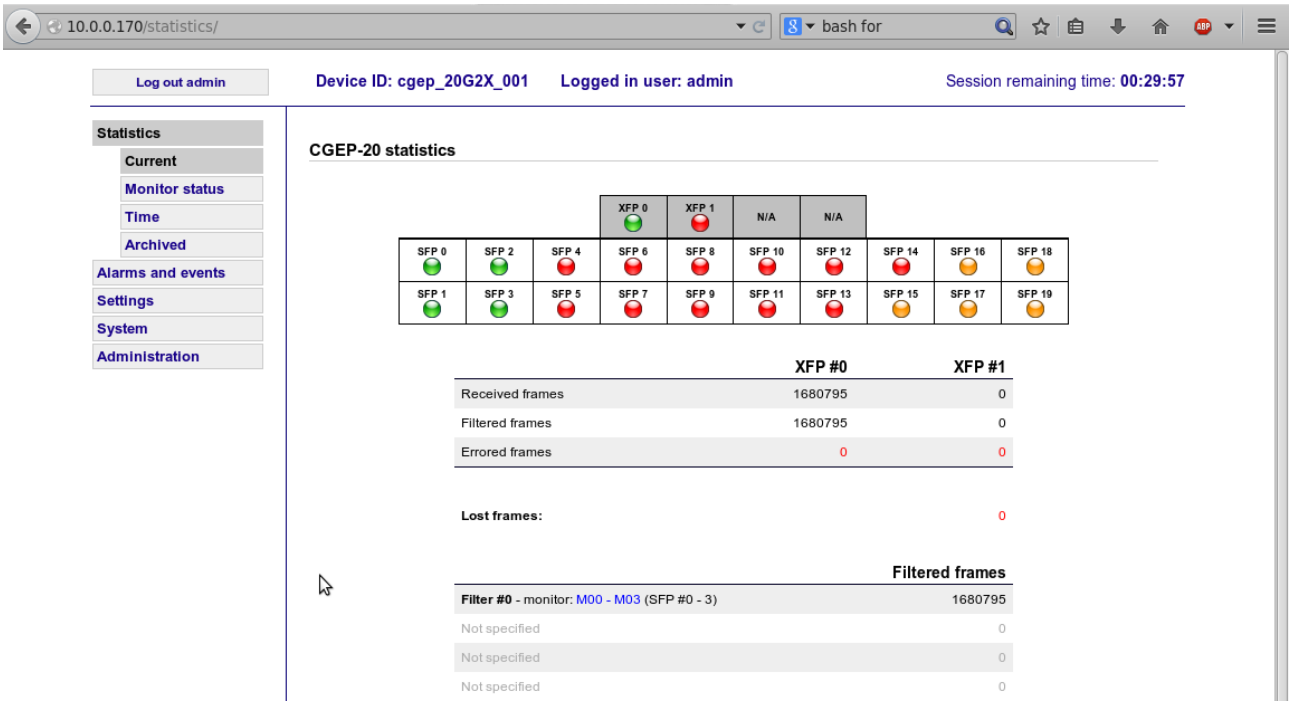
The jumpers on J3 must be closed as stated in 2.6.1 for the built in programmer to work.

The firmware stays resident during reboot, but must be loaded again when doing a cold-boot.

5.2. Web interface

The Web-interface implements a flexible way to configure and manage the application running on the CGEP board.

The screenshot below shows the interface-states (green = link ok, yellow = module plugged, red = no module present), and some basic statistics about the received traffic.


10.0.0.170/statistics/
bash for
Log out admin
Device ID: cgep_20G2X_001
Logged in user: admin
Session remaining time: 00:29:57
Statistics
Current
Monitor status
Time
Archived
Alarms and events
Settings
System
Administration
CGEP-20 statistics
XFP 0
XFP 1
N/A
N/A
SFP 0
SFP 2
SFP 4
SFP 6
SFP 8
SFP 10
SFP 12
SFP 14
SFP 16
SFP 18
SFP 1
SFP 3
SFP 5
SFP 7
SFP 9
SFP 11
SFP 13
SFP 15
SFP 17
SFP 19
XFP #0
XFP #1
Received frames
1680795
0
Filtered frames
1680795
0
Errored frames
0
0
Lost frames:
0
Filtered frames
Filter #0 - monitor: M00 - M03 (SFP #0 - 3)
1680795
Not specified
0
Not specified
0
Not specified
0

6. Firmware Architecture

Interface Cores:

- PCI Express Endpoint block+ (Controller by Xilinx)
    - Device appears as a new network device in the OS
    - Supports busmastering
    - DMA read/write
    - I/O read/write
- 1000 BaseT PCS/PMA + MAC
    - Soft core implemented on GTX transceivers
- 10G XAUI (Controller by Xilinx)
    - Implemented on GTX transceivers
    - Connected to our MAC module
- 10G PCS/PMA (Controller by Xilinx)
    - Implemented on GTH transceivers
    - Connected to our MAC module
- 40G PCS/PMA + MAC (own implementation)
    - 802.3ab compliant implemenation
    - Segmented/Non-Segmented MAC operation mode
    - Simple frame generator
- 100G PCS/PMA + MAC (own implementation)
    - 802.3ab compliant implemenation
    - Segmented/Non-Segmented MAC operation mode
    - Simple frame generator
- DDR3 Contoller
    - DDR3 MIG (Memory Interface Generator by Xilinx)
    - Connected to our Multi-I/O DDR3 Controller module
- MISC
    - MDIO (management)
    - UART for status request (management)
    - System Monitor by Xilinx

Application Cores:

- Monitoring at 10 Gbit/s or 100 Gbit/s link speed
    - Protocol Parsing (QinQ, MPLS – 2 Level, EoMPLS, IPv4 20-60 byte, IPinIP, UDP/TCP, GTP)

    - Filtering
    - Packet Classification
    - Steering
    - Chunker module
    - High precision timestamping
    - PTPv1-Slave module
    - NTP Client module
- Simple traffic generator
    - IPv4 generator
    - GTPv1-U generator

APPENDIX

A.1. Pictures of CGEP_4G4X_1C prototype (100 Gbit/s to 4x10 Gbit/s) platform.

Fig. 1. – Front view of the CGEP_4G4X_1C prototype platform (without).

Fig. 2. – Front view of the CGEP_4G4X_1C prototype platform (with cover)

Fig. 3. – Back view of the CGEP_4G4X_1C prototype platform (with cover).

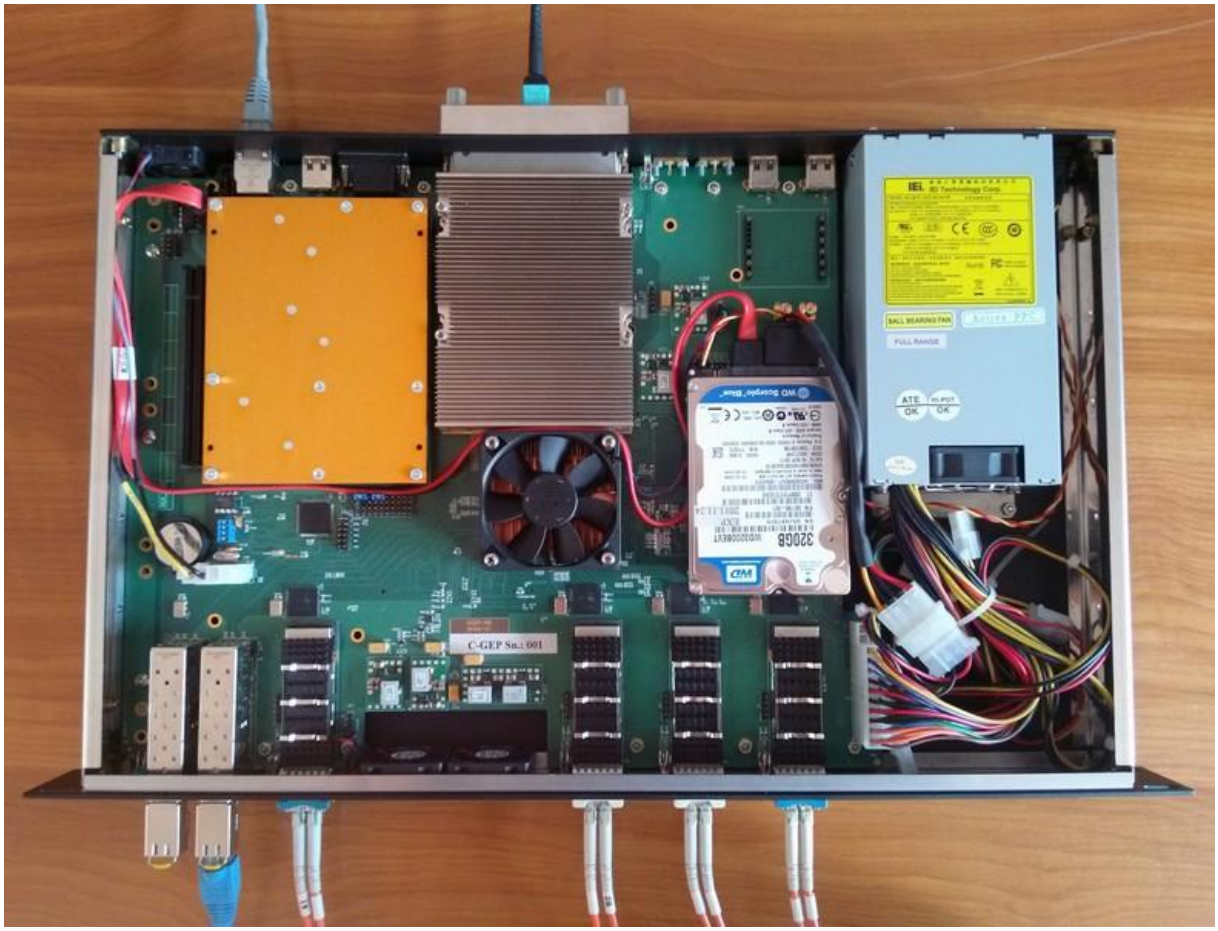


Fig. 4. Top view of the CGEP_4G4X_1C prototype platform (without cover).

A.2. Pictures of CGEP_20G_2X prototype (2x10 Gbit/s to 20x1 Gbit/s) platform.

Fig. 5. – Front view of the CGEP_20G_2X prototype platform (without cover)

Fig. 6. – Front view of the CGEP_20G_2X prototype platform (with cover)

Fig. 7. – Back view of the CGEP_20G_2X prototype platform (without cover)