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Project:

Lutra

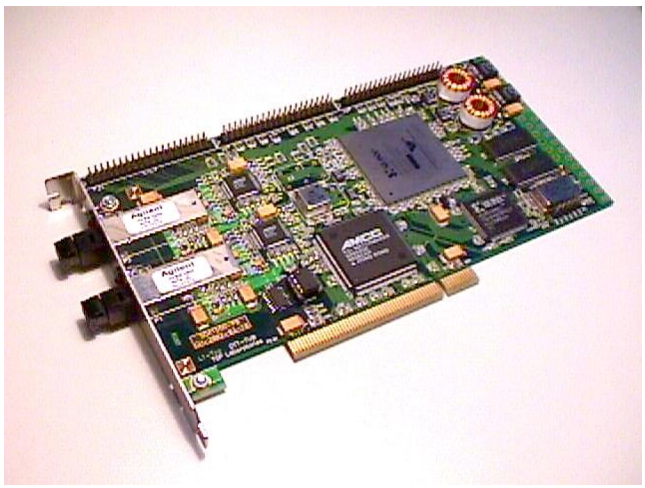
SGA155D STM1/OC3 Telecommunication Interface Card

VOL 1

SGA155D-F1, GH-2002-09-02
CPLD Version 1/Revision 1

Title:

HARDWARE REFERENCE MANUAL



PRODUCTION

(Rev. F1 – october 2002)

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1.1. Features

The ***Lutra*** series SGA155D adapter is a high-performance dual 155Mbit/sec telecommunications adapter designed for use on a standard PCI bus.

The wide range of application fields cover network monitoring, testing, add-drop multiplexing, and terminating SONET/SDH and/or ATM networks.

The adapter features a flexible telecommunications-processor implemented in an FPGA providing maximum performance to applications running on PC or other systems supporting PCI bus.

The firmware for the adapter can be downloaded, allowing dynamic (even in operational state) changes of the functionality, and convenient upgrades reflecting new standards. Non standard operations can also be applied in order to sequencing a conformance test.

Three 40 pins feature connectors are used for connecting other telecom cards, and/or UDMA 66 IDE hard disk drives that allow high speed capture to disk operation for voice, data, or signalling.

SGA155D uses a Virtex FPGA to implement various mapping schemes, and dinamilcally configurable for certain applications such as ATM cell processing, including AAL5 and 3/4 Segmentation and Reassembly (SAR), and DMA by using PCI bus master burst transfers. Separate data paths can be deployed between the network (A/B), the RAM, the hard disk(s), the telecom interface(s), and the PC.

Special features of the card are useful for measurement and streaming applications - such as:

- Monitoring SONET/SDH/ATM networks
- Interface testing
- Protocol and conformance testing
- Latency measurement with 12.86 nsec resolution
- Real-time audio/video streaming
- Implementing transparent WEB cache/proxy

Device driver is available for the vxWorks 5.4 real-time operating system, Windows 9x, 2000, and Windows-XP. The development of driver for DOS is in progress.

1.2. Technical data

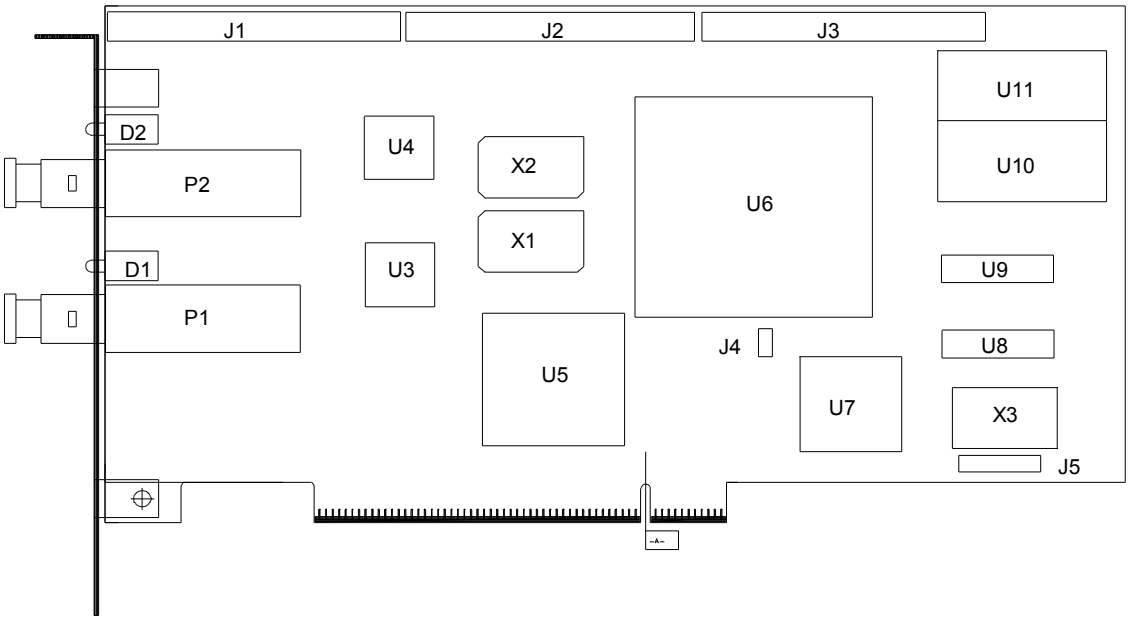
Mechanical	PCI full height, 2/3 long card, with 5 Volts ISA Assembly
- Dimensions	L=210 mm, H=125 mm, W=14 mm
- Weight	0.2 kg (without heat sink)
Host interface	PCI compliant with revision 2.2
- Bus width	32 bits
- Bus type	synchronous A/D/C multiplex
- Frequency	33 MHz nominal
- Throughput	1.056 Gbits/Sec Burst peak cca. 300-500 Mbits/Sec long term
- Powering	5 Volts, consumes 2 A nominal
Optical interface	Dual (A/B) 155 Mbits/Sec SONET STS-3/SDH STM-1
- Connector type	MT/RJ male connectors (shipped with dust cover plug)
- Mode	Multimode
- Transceiver	HFBR5905 InGaAsP LED
-- Center wavelength	1308 nm – typical
-- Optical power out	-15.7 dBm – typical
-- Min. input power	-30dBm (BER < 10E-10)
- Cable	MMF
-- Fiber diameter	125 um
-- Core diameter	62.5/50 um
-- Max. distance	2 km
Memory	2x 512 kBytes SRAM
- Data width	8/16 bits non ECC
- RAM Type	High speed static random access memory
- Frequency	77.76 MHz nominal for synchronous opertion
- Throughput	622/1244 Mbits/Sec long term
- Capacity	Total of 1 Mbytes
- Power	3.3 Volts – nominal
Feature connectors	Triple 40 pins (2x20) Berg type,
- Type	Application defined (IDE/Telecom/Proprietary)
- Default type	E-IDE hard-disk, ATA-4 specification (UDMA-66)
- Bud width	16 bits
- Interface speed	532.8 Mbit/Sec (Ultra ATA/66)
Speaker connector	Two pins Berg type,
- Application	PWM DAC output e.g. for listening voice channel
Frame Processor	Virtex XCV400
- Type	Field Programmable Gate-Array (FPGA)
- Frequency	Running at 77.76MHz nominal, 155.52 MHz with heat sink
- Density	468252 system gates
- CLB array	40x60
- Core	89% of resources available for different applications

1.3. The layout of SGA155D

SGA155D Telecom interface Card is a four layered PCB compliant with the PCI local bus specification revision 2.1 for 33 MHz, 32 bits, full height, 2/3 long card, with 5 Volts ISA Assembly.

The surface and through-hole mounted components are inserted from the top only.

PCB Layers:
- TOP - Wiring
- GND - Ground plane
- VCC - Voltage plane, with islands for 2.5V and 3.3V supply voltage
- BOT - Wiring



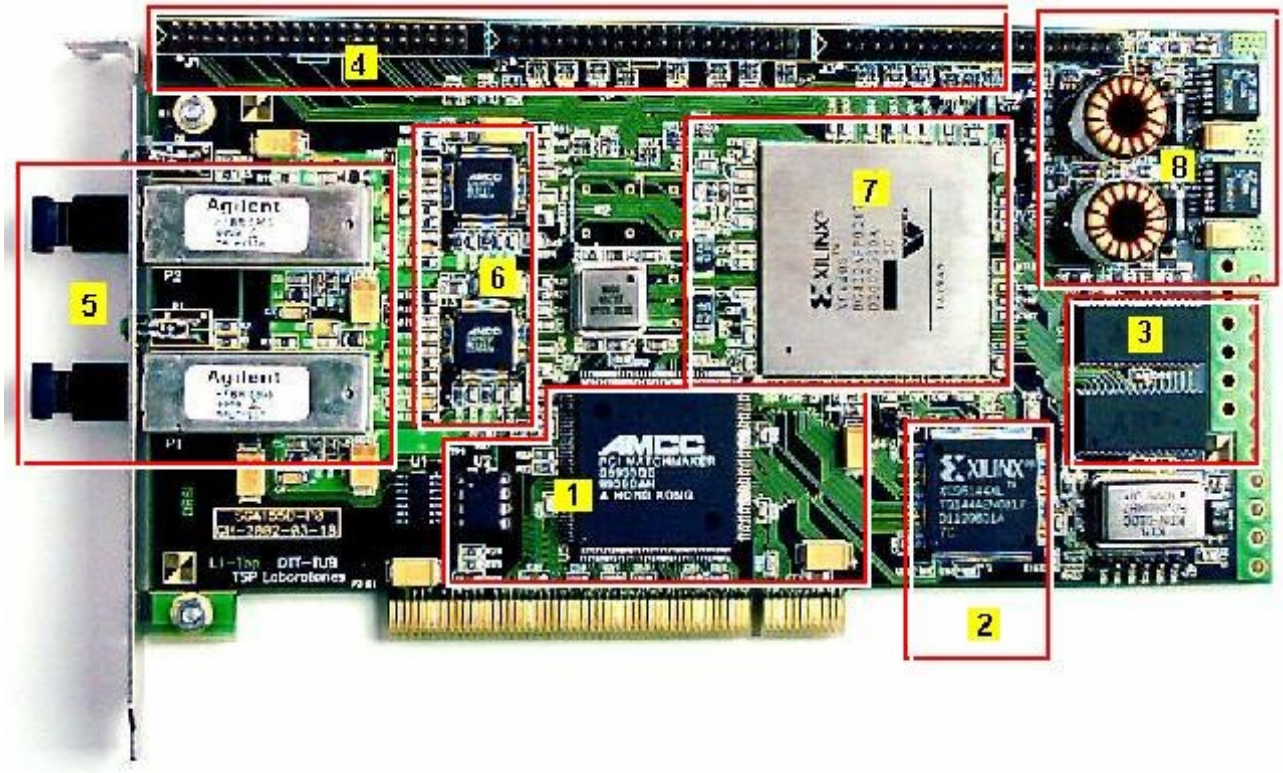
P1. Optical interface “A”
U3. Transceiver “A”
D1. Alarm status LED (Red) “A”
D1. Link status LED (Green) “A”
J1,J2,J3 Feature connectors
-A- Gold plated PCI Edge Connector
U5. PCI controller chip
U7. CPLD chip
U10,U11. Switching Power Supply
X2. 77.76 MHz VCXO

P2. Optical interface “B”
U4. Transceiver”B”
D2. Alarm status LED (Red) “B”
D2. Link status LED (Green) “B”
J4. Speaker connector
J5. JTAG connector
U6. FPGA chip
U8,U9. SRAMs
X1. 77.76 MHz Oscillator
X3. 65,636 MHz VCXO

1.4. The architecture of SGA155D

The SGA155D TELECOM IF CARD consists of eight main blocks:

1. Universal PCI bridge
2. PCI Pass-Through interface (referred as CPLD)
3. SRAM modules
4. Feature connectors
5. Optical interfaces
6. Transceivers
7. Frame/Cell Processor (referred as FPGA)
8. Switching power supply



The detailed description can be found in the following sections.

1.4.1.Universal PCI bridge

This part is a S5933QE PCI MATCHMAKER from AMCC.
The main role is to provide a PCI 2.1 Compliant Master and Slave controller functions including

- Variable width (8/16/32 bits) add-on bus
- Mapping of four block of address space (I/O or Memory, MAP1..3)
- Mailbox support between the host and on-board devices
- FIFO and control for Bus-Mastering DMA transfer

These functions provide data and control path between the host, the Pass-Thru interface and the Frame/Cell Processor.

The PCI identification codes are the following:

Vendor:	DTT-BUTE	Hex: 15C6
Major Class:	Network	2
Minor Class:	ATM	3
Device:	SGA155D	Hex: D155

The card is mapped in the I/O and memory address space as follows

1.4.1.1. I/O Map

Acc.	Base Address	Device	Description
MAP0	Mem ED302000	S5933QE	PCI bridge – controller
MAP1	Mem ED301000	XC95144XL	CPLD Pass thru
MAP2	Mem ED000000	XCV400	Cell processor FPGA/Application Registers
MAP3	IO E400	XC95144XL	CPLD Pass thru repeated in I/O space
MAP4	IO E800	XCV400	Cell processor FPGA indexed into I/O space

The base addresses are given for example only - since they are assigned automatically for plug-and-play (PCI in this case) devices.

See the references section for the details of the I/O map for S5933QE

1.4.2. Pass-thru interface

This block is implemented in a XC95144XL CPLD from Xilinx.

The device is in-system programmable via the standard JTAG port (**J5**), and the configuration data is loaded at the end of the production phase.

As it's name implies - it's main role to provide direct access for the host to the main parts of the card:

- Configuration of the FPGA
- Accessing the FPGA configured as a Frame/Cell-Processor

In normal case, the Frame/Cell-Processor is the central unit controlling the data path on the card. Pass-thru access is used to implement test access points within the frame/cell processor FPGA.

1.4.2.1. I/O Map of the CPLD

Acc.	I/O Base	Device	Description
MAP1,3	**E400**	**XC95144XL**	**CPLD Pass thru**
	+0000	CSR	Board command/status register
R/W	Bit0	Unused	
R/W	Bit1	...XPROG	Pulse to zero to start programming the FPGA
R/W	Bit2	...XWRITE	Enable writing FPGA configuration data
R/W	Bit3	...XCS	Select the FPGA for programming
R/W	Bit4	...Unused	
R/W	Bit5	...Unused	
R/W	Bit6	...XINIT	Delays the FPGA configuration startup
R	Bit7	...XDONE	Signals that FPGA configuration completes
R/W	Bit8..31	...unused	
	+0004	IDR	32 bits Identification register
R	Bit0..7	...CPLDREV	Revision number
R	Bit8..15	...CPLDVER	Version number
R	Bit16..31	...DEVID	Device ID (should be 0xD155)
R/W	+0008..00EF	FPGA xxxx	Cell Processor/Application defined test access
W	+00F0	XDATA	Write Xilinx configuration data here
R/W	+00F8	TEST	32 bits Test register, returns bitwise NOT

1.4.3. Feature connectors

There are three 40 pin connectors (**J1**,**J2**,**J3**) on the card. The function of these connectors are application defined, and can be programmed in the FPGA.

It can be used to communicate with other SGA, Lutra, or Cellpicker series cards's - forming a back-plane with 1 Gbit/Sec simplex throughput.

Secondary roles can also be assigned to the interfaces.
As an IDE interface, it allows the user to attach IDE Hard-Disk drive(s) to the card.
The main role of an attached HDD is to store and retrieve a large amount of voce, data, or signalling information or filtered cell data for off-line analyzis. The speed depends on the type of the hard disk drive.

1.4.3.1. Feature connector pin-out

Proprietary telecom interface

RST	1	2	**GND**
F0	3	4	S0
C0	5	6	D0
C1	7	8	D1
F1	9	10	S1
C2	11	12	D2
F2	13	14	S2
C3	15	16	D3
F3	17	18	S3
GND	19	20	**N/C** (key)
DIR	21	22	**GND**
CLK	23	24	**GND**
F4	25	26	**GND**
C4	27	28	D4
F5	29	30	**GND**
C5	31	32	D5
F6	33	34	**GND**
C6	35	36	D6
C7	37	38	D7
F7	39	40	**GND**

Standard IDE HDD connector

RST	1	2	**GND**
D7	3	4	D8
D6	5	6	D9
D5	7	8	D10
D4	9	10	D11
D3	11	12	D12
D2	13	14	D13
D1	15	16	D14
D0	17	18	D15
GND	19	20	**N/C** (key)
DRQ3	21	22	**GND**
IOW	23	24	**GND**
IOR	25	26	**GND**
IOCHRDY	27	28	BALE
DACK3	29	30	**GND**
IRQ14	31	32	IOCS16
A1	33	34	**GND**
A0	35	36	A2
CS0	37	38	CS1
ACT	39	40	**GND**

1.4.4. On-board memory

There are two 512 kBytes SRAM on the card. It can be used as two separate 8 bits wide memory or a single 16 bits if they are combined together. It is application dependent how to organise them. They are mapped into the hosts memory space (MAP2), and also available indexed into the I/O space (MAP4) for DOS applications.

The memory can play the following roles:

- Elastic store in telecom applications
- FIFO for bus mastering data into the PC
- Cache for disk access
- Stores VPI/VCI states for SAR in ATM applications

All of these functions can be applied in the same application simultaneously.

1.4.5. Optical interfaces

These parts are HFBR5905 from Agilent Technology.
Multi-Mode optical cable assembled with MT/RJ connector can be attached to these parts.
Single-Mode optical lines can be monitored by using 10 dB optical attenuator or 9:1 splitter.

The 155 Mbits/sec serial data is processed by the transceivers.

1.4.6. Transceivers

This 155 Mbit/Sec transceiver with clock and data recovery is manufactured by AMCC.
The part number is S3032.

It provides
- duplex bit-serial 155 Mbit/sec STS3/STM1 data stream to the Optical Interface
- Integrated Clock/Data recovery and clock synthesis
- Parallel byte-wide system interface to the frame/cell processor FPGA, clocking at 19.44MHz

The main role is to provide serial to parallel and parallel to serial data conversion, line coding/decoding, clock/data recovery, and some basic functions of framing (provides FP frame pulse, and accepts OOF status signal).

1.4.7. Frame/cell processor FPGA

The core of the architecture is a very large scale and flexible device - XCV400 FPGA from Virtex.

The main characteristics:
- 468252 system gates
- 40 row by 60 column CLB array - 4 logic blocks in each
- 316 user programmable I/O pins
- 82 kbits of RAM in CLB's (BlockRAM)
- 153 kbits of RAM separately (SelectRAM)
- Zero skew internal clocking up to 200 MHz

The device can be programmed on-the-fly from the host by using the Pass-Through interface.

User I/O pins are connected to the other on-board devices.

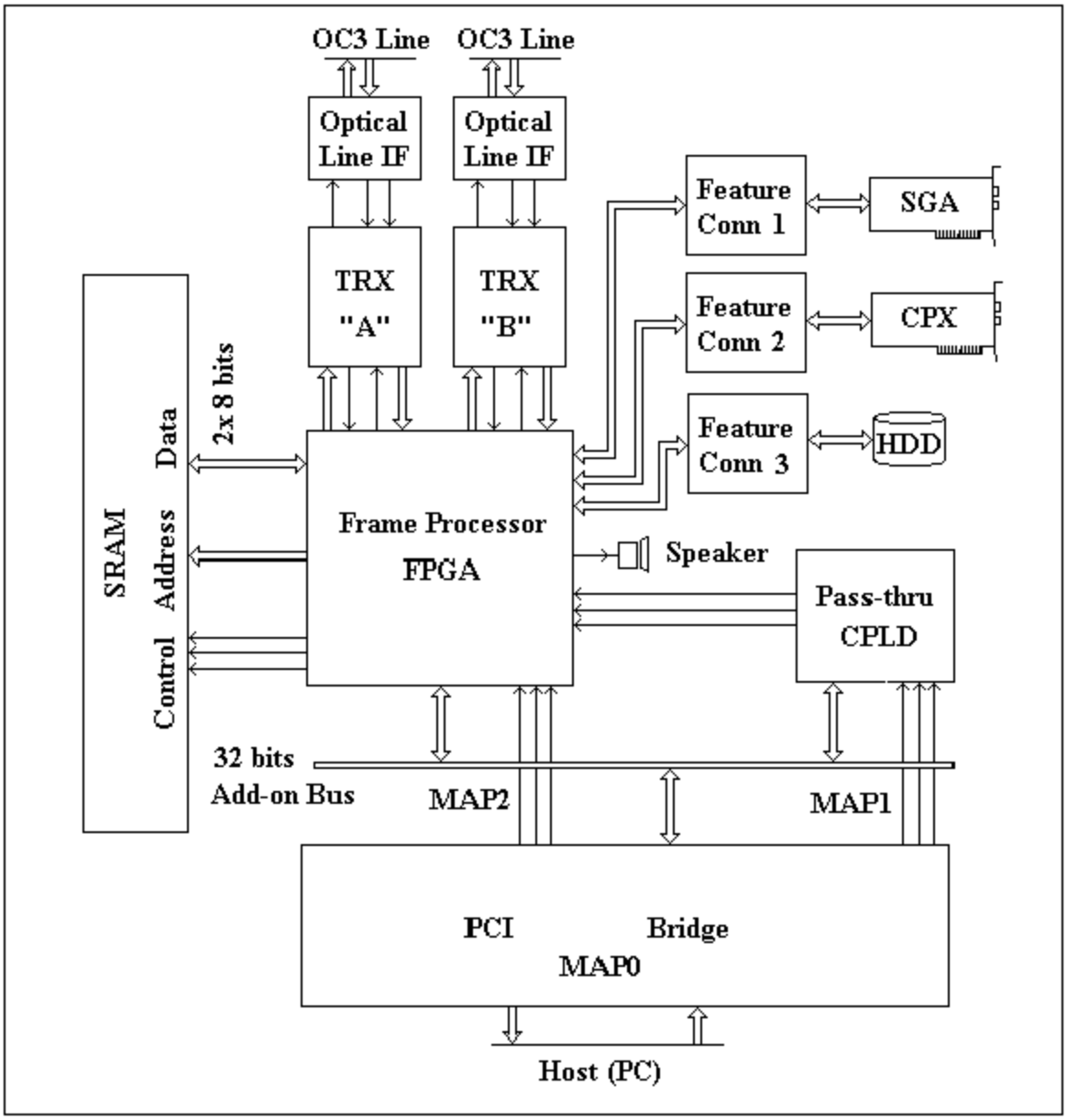
The proposed roles of the device are the following:

- Various mapping/multiplexing voice/data/signalling channels
- Synchronous interface to the SRAM, and R/W buffers
- IDE controller supporting 16 bits wide DMA transfer
- Host communication through the PCI bridge (Bus mastering)
- Data path unit connecting the parties above

1.4.8. Switching power supply

The devices on the card require different voltage supplies:
+5V - Optical Interface, PCI bridge
+3.3V - S/UNI, FPGA I/O voltage, CPLD
+2.5V - FPGA core voltage
We generate 3.3, and 2.5 volts by using switching power supplies from the 5 Volts provided by the PC.

1.5. Operation of SGA155D



The operation of SGA155 card can be followed on the figure above – containing the block diagram.

1.5.1. Power on

After the installation of the card, and powering the PC, the board is brought up in it's un-configured state.

This status is signalled by the LED's on the card as follows:

- Link status LED (green) lit steady
- Alarm status LED (red) lit steady

The PC's BIOS should enumerate the card as a PCI Network Adapter. Also, if a plug and play OS is installed on the PC, the OS should recognise the card as a PCI ATM Network Adapter. The installation of the device driver is started automatically.

1.5.2. Configuration

A device driver will configure the FPGA on the card for the particular purpose.
The configuration data is passed from the host through the CPLD to the FPGA.

The configured state is signalled by the LED's on the card as follows:
- Link status LED (green) lit only if the fiber is connected to card, and lit.
- Alarm status LED (red) lit only if the pre-programmed alarm conditions are met.

1.5.3. Application

Typical application uses the FPGA to implement the main functions - as described in Volume 2. The frame/cell processor can access all the board’s resource such as:

- Transceiver’s bus
- The feature connectors
- Memory (SRAM)
- Capable to bus-master data to the host

1.5.3.1. Reception

Byte parallel data from the transceiver is fed into the FPGA. STM1 frame detection algorithm is implemented first to provide OOF (Out Of Frame alignment) status information, and to feed back to the transceiver. Parallel data with the correct frame pulse (FP) is passed to the FPGA’s application arena for further processing.
The optional scrambler is the part of the FPGA core.

The application arena should implement the functions to access data/voice/signalling mapped in the STM1 level SDH.

These data/voice streams or signalling messages can then be passed to the SRAM, to the Feature connectors, to the PC or to all of them using separate data path at the same time.

1.5.3.2. Transmission

The FPGA core implements basic STM1 framing including an optional scrambler.
The byte parallel data is sent to the transceivers.

Multiple, and concurrent (even priority) sources can excite the transmitter section such as:

- the SRAM buffers filled with test patterns (frame/cell)
- the hard disk – AND/OR - the back-plane through the feature connectors
- the host, using Bus Mastering DMA

Mapping data/voice or signalling channels are implemented in the FPGA, therefore very exotic schemes can be applied. Classic telecom multiplexing, packet over SONET (POS), or ATM applications are trivial.

Precise timing can be achieved at the resolution of 12.86 nSec.
Complete - timed - playback of a previous records can also be implemented.

1.5.3.3. Clocking schemes

There are three crystal oscillator installed on board:

- 77.76 MHz commerce oscillator +/- 50 ppm for standard applications
- 77.76 MHz VCXO that is pullable +/- 150 ppm for special application such as interface testing, WAN clocking, synchronising to GPS timing source, etc…
- 65.536 MHz VCXO for PDH applications/testing

Recovered clocks (from the network) are also available in the FPGA's application arena. Therefore, exotic clocking schemes are at our hand.

1.6. References

Agilent technologies	http://www.agilent.com
- HFBR5905	ftp://ftp.agilent.com/pub/semiconductor/fiber/hfbr5905.pdf
AMCC	http://www.amcc.com
- S5933	http://www.amcc.com/pdfs/pciprod.pdf
- S3032	
Xilinx	http://www.xilinx.com
- XCV400	http://www.xilinx.com/partinfo/ds003.pd f
- XC95144XL	http://www.xilinx.com/partinfo/95144xl.pdf

1.7. Revision Notes

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1. Identification
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The PROTOTYPE (P0) can be identifed as printed on both top and
bottom of the PCB:

   SGA155D-P0
   GH-2002-03-18

The FINAL (F1) product can be identifed as printed on both top and
bottom of the PCB:

   SGA155D-F1
   GH-2002-09-02

2. Problems and solving
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2.1 Unconfigured state
......................

In the unconfigured state, all LEDs should lit steady.
They lit at random instead.

In the material list U1 appeared to be a 74HC04.
74HCT04s have to be inserted instead.
The material list is corrected for the F1 PCB accordingly.
```

2.2 Transceiver section

The SD (Signal Detect) signal does not reflect the state of the optical input.

Transceivers P1 and P2 have to be terminated by 100s ohm on their SD pins. Also, R5 and R8 (750 ohm) have to replaced to 33 ohm.

Small 100 ohm resistors have to be soldered between pad 1 and 3 manually for prototype cards.

The schematic and pcb diagrams, and the material list have been corrected accordingly for F1.

3. Prototyping results

After the modifications described in 2., the prototype appeared to be fully operational.
In brief:

- The board fits correctly in the PC
- 2.5 and 3.3 Volts power supplies are in range
- It is functional as PCI target device well (CPLD passed)
- The FPGA can be configured for test operations
- Static RAMs appeared OK
- Transceivers are operable
- Feature connectors can be driven

(See the manufacturers test log for details)