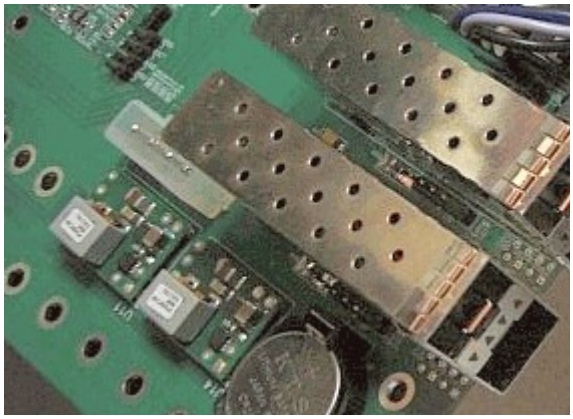
CBOARD

Rev.3.

Scalopes evaluation platform

for high speed networking



REFERENCE MANUAL

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ETIK KKK

Contents

1. Introduction 

1.1 What is CBOARD?

CBOARD is a multi-core, power sensitive, high speed networking evaluation platform.

Wide range of applications can be deployed on this multicore platform:

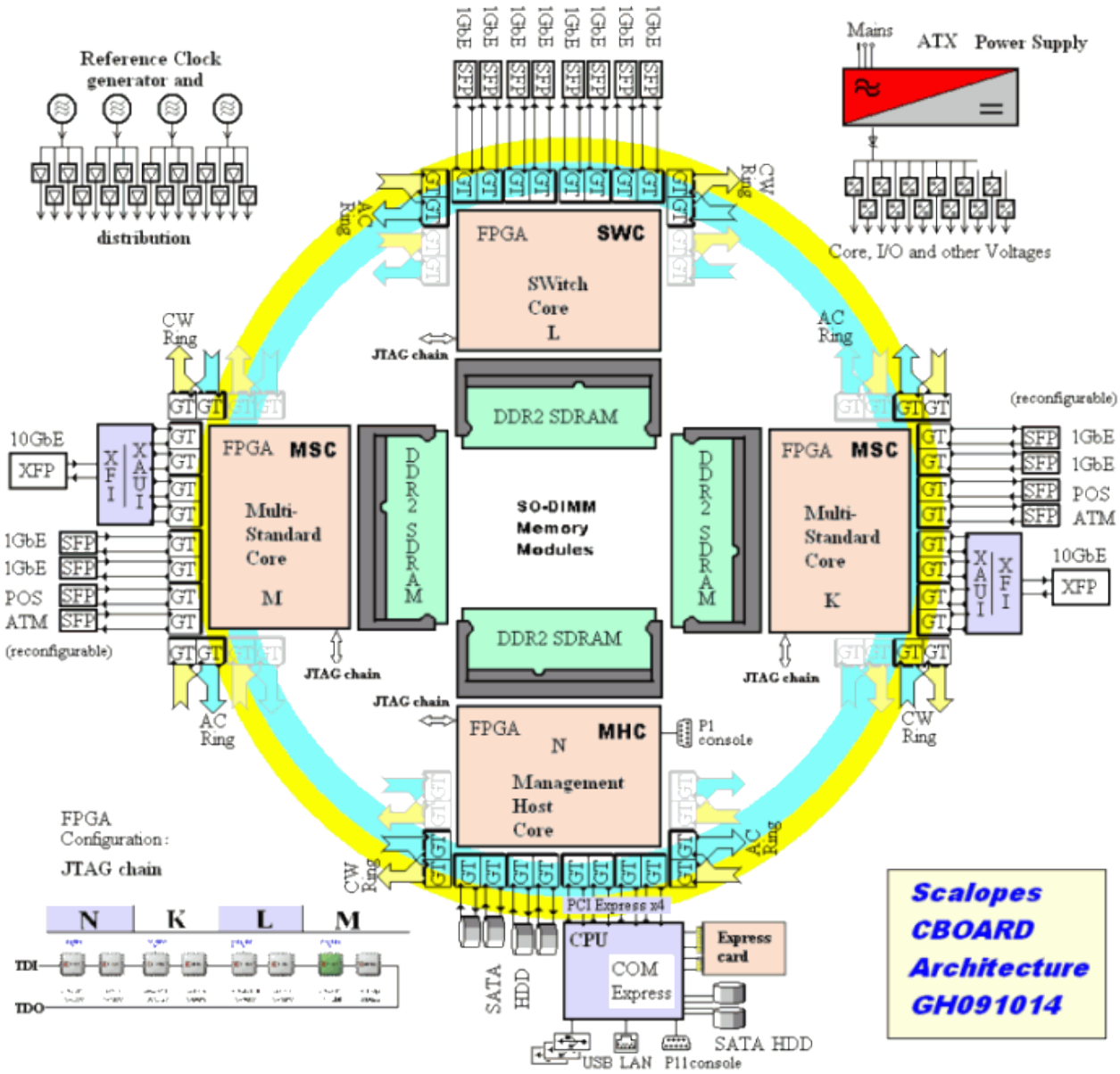
1. MONITORING - TRAFFIC MIX
    1. Traffic mix definition
    2. Measuring traffic mix, important attributes
2. DEEP PACKET INSPECTION
    1. Signature based application identification
    2. Statistical analysis by numerical properties
    3. Analysis by Behavior and Heuristics
    4. Chi-square classifier
3. IMS SIP PLATFORM
4. ROUTING
5. VIDEO-TRANSCODING
6. MEDIA GATEWAY
7. FIREWALL
8. TRAFFIC GENERATOR

Application features:

- 64 bit Timestamp with 4/8 nsec resolution,
- lossless packet capture limited only by host PC's speed and resources,
- header-only capture: configurable protocol layer depth decoded by hardware on-the-fly,
- fully PCAP/WINPCAP compliant interface,
- parameterized line speed capable packet/flow generator for active measurements,
- RFC 2544 tester implementation

1.2 What is on-board?

The figure below shows the major on-board components.



1.2.1 Architecture

The SCALOPES C-board occupies a standard 1U x 19 inch rack mount case, with active cooling on ATX style power supplies, and passive cooling on board.

Network interface connectors are mounted on front; management, and mains connectors are on the rear panel.

The main part of the hardware is the FPGA ring, containing four FPGAs (Virtex 5, XC5VLX110T).

The external interfaces (SFP, XFP and PCI-E slots) connect to the FPGA's GTP dual ports, which allow high-speed communication between interfaces. Further variation of interfaces (Gigabit fiber, 10/100 Ethernet, STM-1 optic etc) is possible by using SFP module receivers.

1.2.2 Interfaces

Front mounts:

- 1 USB host connector
- 2 XFP module receptacle for 10 Gbps Ethernet,
- 16 SFP module receptacle for 1G/100M/10 Ethernet (half of them are available for Multistandard / Multirate applications).

Rear mounts:

- 1 USB host connector (+1 internal for booting a pendrive, and 4 more on pin headers),
- 1 RJ45, 10/100 Ethernet for management LAN,
- 1 DSUB connector for VGA monitor
- 2 DB9 for RS232 console connection.
- 1 PS/2 Keyboard.
- 1 PS/2 Mouse.
- 1 ExpressCard receptacle

Internal mounts:

- 4 SODIMM200 receptacle for 1.8V DDR2 SDRAMs,
- 1 Express Card module receptacle,
- 1 COM (Computer On Module) Express receptacle.

1.2.3 The FPGA-ring

The FPGA-based networking cores are tied onto a Gigabit bi-directional ring, implementing 2x14 Gbps backplane capacity (ClockWise, and AntiClockwise). This bi-directional ring is made especially visible in the architectural figure.

In addition, a TDM local bus is available for handling exceptions, traps, and out-of-band signaling-data, as well as clock synchronization. The physical and logical connection between the interfaces is defined by the FPGA firmware ensuring the hardware's flexibility. The current firmware is stored on flash memory connected to the chips: they load as soon as the hardware starts.

There are four FPGA cores on the board: one Management Host Core (MHC), two Multi-Standard Cores (MSC), and one Switch Core (SWC).

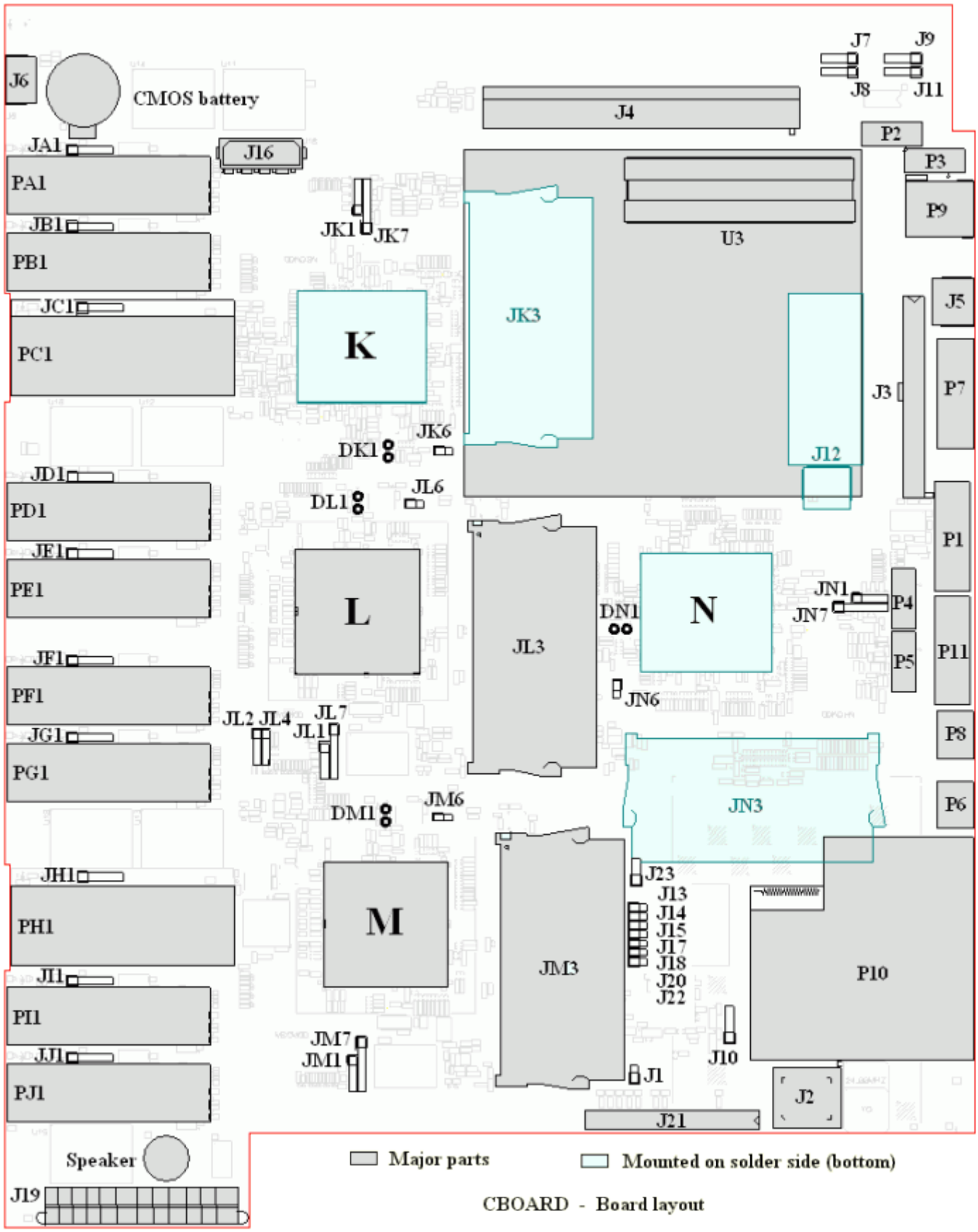
- The Management Host Core (**MHC** Core N) can be used to connect the ring to a management PC (COM Express module) for managing the C-BOARD and terminating network services. At least it can be a control prcoessor if the COM-Express module is omitted.
- The 2x Multi-Standard Cores (**MSC** Core K and M) can be used as media Gateways and to integrate legacy network links into a modern core network. SDH based TUG/POS/ATM carriers are supported.
- The Switch Core (**SWC** Core L) is a generic part of the ring - implementing router functions beyond tagged switching, and MPLS.

Each core has a good load of RAM installed as DDR2 SODIMM module. Its purpose is application defined. Switch matrix, flow-CAM, QOS queues can use it.

1.2.4 Computer On Module

The management computer of the C-board is implemented using COM Express Type-2 (or higher) child board, running Linux operating system.

1.3 Board Layout - connectors and jumpers



1.3.1 J1 jumper - BIOS disable

Closing J1 disables the COM-Express on-board BIOS, and enables CBOARD's - designated J2. Default is open.

1.3.2 J2 - CBOARD BIOS receptacle

J2 can accomodate an Intel (R) 82802xx compatible Firmware Hub, a CMOS flash device containing optional CBOARD's BIOS. It can be enabled closing J1. Device is not installed by default.

1.3.3 J3 - IDE (PATA) connector

Type-2 COM-Express modules (designated as U3) should implement an UDMA100 IDE controller. A PATA hard disk, and/or a CD-ROM drive can be attached to J3.

1.3.4 J4 - PCI Express Graphics (PEG)

A PCI Express x16 graphics adapter can be indtalled in J4. Before using PEG port, it has to be enbled by closing J22.

1.3.5 J5 - Rear mounted USB0 connector

Type-2 COM-Express modules (designated as U3) may implement several USB 2.0 ports. Standby powered USB0 at J5 is mounted on the rear panel.

1.3.6 J6 - Front side USB1 connector

USB1 at J6 is mounted on the front panel of CBOARD. It is powered from ATX main rails.

1.3.7 J7,J8,J9,J10,J11 - Pin-headers USB2,3,5,6,7

USB2,3,5,6,7 are routed to internal pin headers. USB6 is routed to the ExpressCard receptacle P10 too.

The pinout of USB pin headers:

1 - VCC; 2 - USB-; 3 - USB+; 4 - GND

1.3.8 J12 - Internal USB4 connector

USB4 at J12 is internally mounted on the solder side (bottom) of CBOARD. It is powered from ATX standby rail, and can accomodate a generic pen-drive sized USB device.

1.3.9 J13 jumper - Power on from SuperIO

Close J13 to include SuperIO into ACPI power on sequence, such as Power-On from keyboard. The power button has to be connected to J18, and is J14 disconnected in this case. Default is open.

1.3.10 J14 - Power button to COM-Express

Connect the power button to J14 for COM-Express Host (default). If the host module at U3 is not installed, a normal on/off power switch has to be connected to pin 2 of J14 and pin 2 of J15.
If ACPI involves the SuperIO chip, the power button has to be connected to J18.

1.3.11 J15 jumper - ATX power on from SuperIO

Close J15 to source the ATX PSON signal from the Superio. Default is open.

1.3.12 J16 - Extra power feed to PEG

Use J16 to feed extra power to PEG if necessary. Default is N/C.

1.3.13 J17 jumper - ATX power on from COM-Express

Close J17 to source the ATX PSON signal from the COM-Express host module. Default is close.

1.3.14 J18 - Power button to SuperIO

Connect the power button to J18 if ACPI involves the SuperIO chip. Power button is connected to J14 by default.

1.3.15 J19 - ATX Power connector

Connect the ATX power supply to J19.
The pinout of the ATX style connector:

13	VCC3V3	1	VCC3V3
14	VCC-12	2	VCC3V3
15	GND	3	GND
16	#PSON	4	VCC5
17	GND	5	GND
18	GND	6	VCC5
19	GND	7	GND
20	N/C	8	PWGOOD
21	VCC5	9	VCC5SB
22	VCC5	10	VCC12
23	VCC5	11	VCC12
24	GND	12	VCC3V3

1.3.16 J20 - Reset button

COM-Express module can be reset by using a button connected to J20. This is the default.

1.3.17 J21 - Floppy disk drive connector (FDD)

SuperIO chip contains an FDC. Use J21 to connect an FDD.

1.3.18 J22 jumper - Enable PEG

Close J22 to enable PCI Express Graphics (PEG) if an appropriate graphics card is installed at J4. Default is close.

1.3.19 J23 - FPGA reload

This multifuctional pin header is used to control the FPGA startup behaviour.

- Close pin 2 and 3 to force FPGA reload from platform flash if the COM-Express host module is reset.
- Connect the reset button to pin 1 and 2 if the host module is not presnt. The power switch (not a push-button) has to be connected to pin 2 of J14 and pin 2 of J15.
- Leave it open (default) for POR only reconfiguration.

1.3.20 JA1,JB1,..JJ1 - ICSP Pin-headers

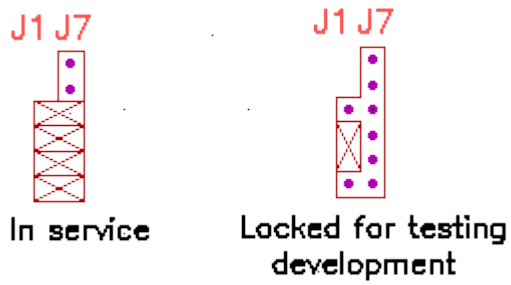
In-system programmable Microchip (R) interface controllers can be reprogrammed through these headers using ***Brenner-9*** type programmers.
Defaults (COREA and COREC firmware) are preloaded.

The pinout of ICSP pin headers:

1 - VPP; 2 - VCC3V3; 3 - GND; 4 - ICSPDAT 5 - ICSPCLK

1.3.21 JK1,JK7,JL1,JL7... - JTAG chain

Four FPGAs and their Platform flash counterparts are organized into a flexible JTAG-chain. Each block can be bypassed by jumpers, and can be individually programmed through the pin header. See the figure below.



Jx1		Jx7
	1	VCC3V3
	2	GND
1	Board TCK	3 TCK
2	DO to borad	4 DO from flash
3	DI from board	5 DI to FPGA
4	Board TMS	6 TMS

1.3.22 JK3,JL3,JM3,JN3 - DDR2 RAM SODIMM receptacles

Each FPGA block has its own DDR2 RAM module.
A Xilinx COREGEN tested Micron Semiconductor part MT4HTF3264HY-667D3 or similar 256MB DDR2-667 RAM can be installed here.

1.3.23 JK6,JL6,JM6,JN6 jumper - FPGA pullup

Close this jumper to enable a weak pullup during the configuration of FPGA. Default is close.

1.3.24 P1 - MHC Console port (N block)

Use this right angle DB-9 male connector to access MHC console at 115200,8,N,1.
This serial communication port is visible as RS232 (assigned to stdin, and stdout too) in the ***coren_console_hub*** example design for Xilinx XPS and SDK using microblaze.

The pinout of MHC console:

1	DCD	6	DSR
2	RXD	7	RTS
3	TXD	8	CTS
4	DTR	9	RI
5	GND		

1.3.25 P2,P3 - COM-Express SATA0, and 1

Type-2 COM-Express modules (designated as U3) may implement several SATA (Serial ATA HDD) ports. SATA0 and 1 are available on CBOARD.
Note that IDE HDDs can also be connected to CBOARD using J3.

1.3.26 P4,P5 - MHC module SATA0, and 1

COREN cores for MHC may implement SATA (Serial ATA HDD) ports. Connect SATA HDDs to P4, and P5 for MHC cores.

1.3.27 P6 - PS/2 Mouse

PS/2 mouse can be connected to the rear mounted P6 connector. This feature is available for COM-Express+SuperIO configuration, or for LPC bus mastering MHC cores.

1.3.28 P7 - VGA D-SUB connector

VGA monitor can be attached to CBOARD if a Type2 COM-Express module is installed at U3.

1.3.29 P8 - PS/2 Keyboard

PS/2 keyboard can be connected to the rear mounted P8 connector. This feature is available for COM-Express+SuperIO configuration, or for LPC bus mastering MHC cores.

1.3.30 P9 - RJ45 UTP/STP LAN connector

Type-2 COM-Express modules (designated as U3) should implement a 10/100 Mbps Ethernet NIC. LAN cable can be attached to P9 using 8 pins RJ45 plug.

1.3.31 P10 - ExpressCard receptacle

P10 can accomodate ExpressCards having EC/34 or EC/54 form factor. It consumes one PCI Express lane, and one USB port from the COM-Express resoures.

1.3.32 P11 - Console port for COM-Express host

Use this right angle DB-9 male connector to access Host console at 115200,8,N,1.
This serial communication port is visible as COM1 from the COM-Express host running Windows, or /dev/ttyS0 under Linux.

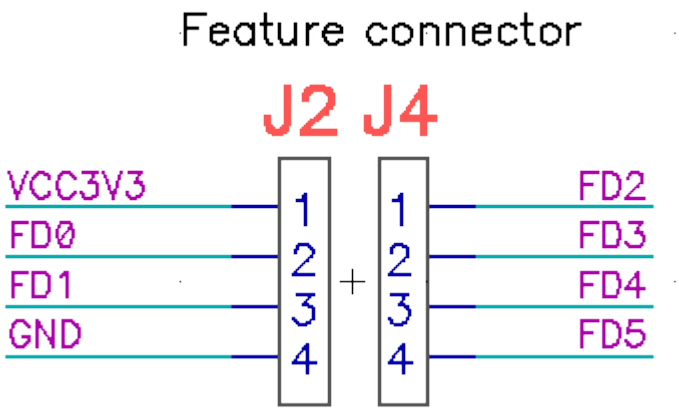
1.3.33 PA1,PB1,...PJ1 - Network interface SFP/XFP receptacles

The following table shows the Network interface, SFP/XFP cage, controller firmware, and FPGA core assignments:

No.	Cage	Controller	FPGA
0	JA1 SFP Lower	COREA	COREK
1	JA1 SFP Upper	COREA	COREK
2	JB1 SFP Lower	COREA	COREK
3	JB1 SFP Upper	COREA	COREK
4	JC1 XFP	COREC	COREK
5	JD1 SFP Lower	COREA	COREL
6	JD1 SFP Upper	COREA	COREL
7	JE1 SFP Lower	COREA	COREL
8	JE1 SFP Upper	COREA	COREL
9	JF1 SFP Lower	COREA	COREL
10	JF1 SFP Upper	COREA	COREL
11	JG1 SFP Lower	COREA	COREL
12	JG1 SFP Upper	COREA	COREL
13	JH1 XFP	COREC	COREM
14	JI1 SFP Lower	COREA	COREM
15	JI1 SFP Upper	COREA	COREM
16	JJ1 SFP Lower	COREA	COREM
17	JJ1 SFP Upper	COREA	COREM

1.3.34 JL2, JL4 - Feature connectors

The feature connector of SWC CORE (L) has the following pinout:



1.4 Conformity

CBOARD aims the following Standards/Recommendations:

XFP	**10 Gigabit Small Form Factor Pluggable Module** SFF Committee INF-8077i 10 Gigabit Small Form Factor Pluggable Module
10GE	**10 Gbps Ethernet (Optical)** IEEE Std 802.3 Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications
SFP	**Small Formfactor Pluggable Transceivers** SFF Committee INF-8074i Specification for SFP Transceiver SFF Committee SFF-8075 Specification for PCI Card Version of SFP Cage SFF Committee SFF-8472 Specification for Diagnostic Monitoring Interface for Optical Xcvrs
...SDH	**Synchronous Digital Hierarchy** ITU-T G.707/Y.1322 Network node interface for the synchronous digital hierarchy (SDH)
...GBE	**Gigabit Ethernet (Optical/Copper)** IEEE Std 802.3 Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications
PCIE	**PCI Express** PCI-SIG PCI Express Base Specification Revision 1.0a PCI-SIG PCI Express Card Electromechanical Specification Revision 1.0a
DDR2	**Dual DataRate II. SDRAM and Modules** JEDEC JESD79-2D DDR2 SDRAM SPECIFICATION JEDEC No.21C 4.20.11 200-Pin DDR2 SDRAM Unbuffered SODIMM Design Specification. (Item #2017.10) Release No. 17
FC	**xx pins Feature Connector**
...PDH	ITU-T G.703 Physical/electrical characteristics of hierarchical digital interfaces (.9 with passive feature card)
IDE	NCITS 361-2002 AT Attachment with Packet Interface - 6 (ATA/ATAPI-6/UDMA5/UDMA100/UATA100 interface)
SATA	INCITS T13/e03104r0 Serial ATA: High Speed Serialized AT Attachment

1.5 PCB Technology

1.5.1 Overview

CBOARD lays on a six layered FR4 PCB with SMD components on both sides, through hole, and heavier componets are inserted on top.

Its form factor allows to fit in a stabndard 1U rackmount case.

The following chapters describe the layer stacking, the metric of routing/plane copper layer, etc...

1.5.2 Layer stacking

The table below shows the layer structure of the board, and the names of the corresponding GERBER files.

1	17.5 um Cu	GPLANAR1_L1_TOP.gbr
	2x100 um prepreg	-
2	35 um Cu	GPLANAR1_L2_GND.gbr
	350 um Core	-
3	35 um Cu	GPLANAR1_L3_MID1.gbr
	2x100 um prepreg	-
4	35 um Cu	GPLANAR1_L4_VCC.gbr
	350 um Core	-
5	35 um Cu	GPLANAR1_L5_MID2.gbr
	2x100 um prepreg	-
6	17.5 um Cu	GPLANAR1_L6_BOT.gbr

1.5.3 Metric

The narrowest traces are 6 (six) mils wide. The clearence (TT,TP) is 6 (six) mils.

Via's are all 'through' types, and covered by solder mask coating on both sides. All potential test points are available on SMD pads.

The Solder Mask Annual Ring is 2 mils (for Non-Solder-Mask-Defined pads too).

Smallest vias are 20/10 mils. All plane connections are direct type, for better cooling and conducting performance.

1.5.4 Controlled impedance lines

There are several lines used to carry very high speed data. Sigle ended lines have 50 ohm nominal impedance. Differential lines are 100 ohms. The table below shows the metric of the lines for the layer stacking above.

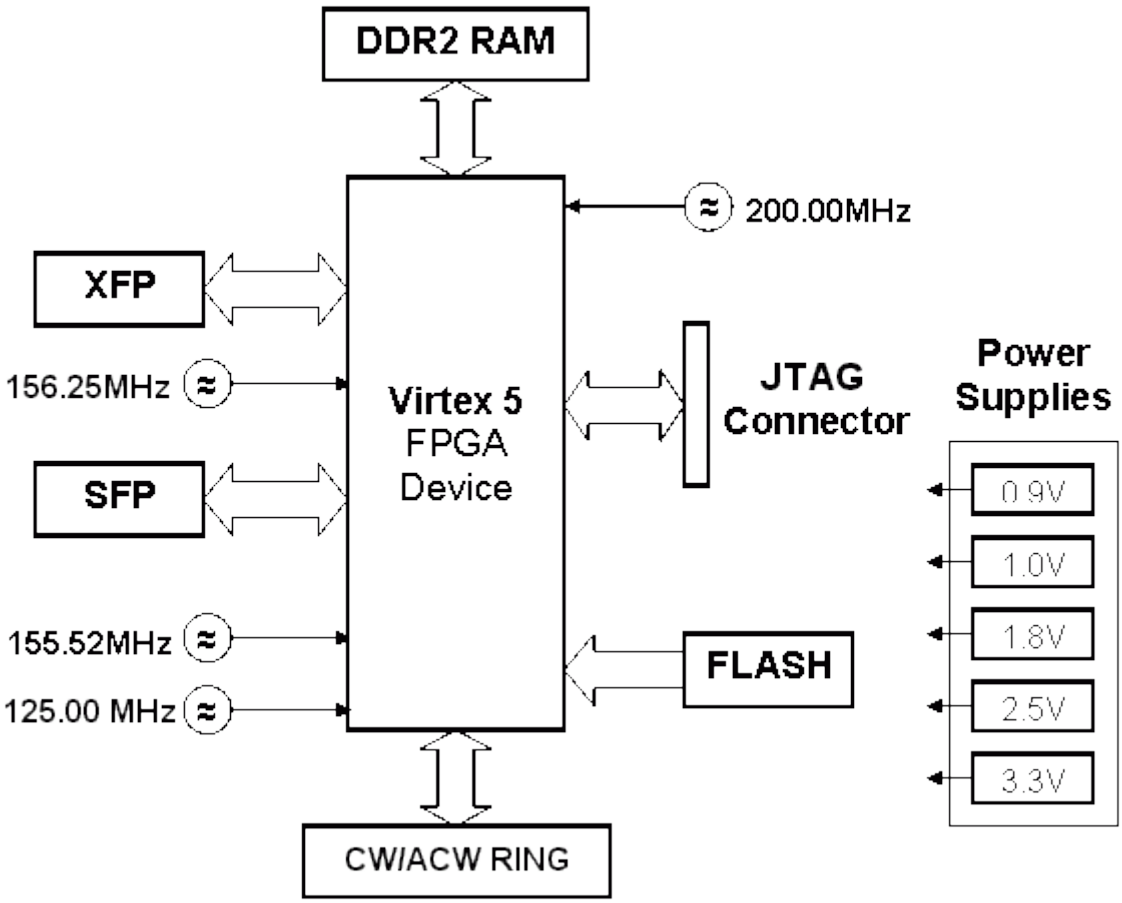
Layers	Type	Metric	Zo
1,6*	Coated surface uStrip	12 mils single trace	53.8
1,6*	Differential, edge coupled Coated surface uStrip	8 mils trace-pair, 7 mils gap	103
1,6*	Differential, Coplanar Waveguide with Ground	8 mils trace-pair, 7 mils gap, GND edge at 6 mils	99
3,5**	Offset Stripline	6 mils single trace	54
3,5**	Differential, edge coupled Offset Stripline	6 mils trace pair, 10 mils gap	98

* Layer 6 has grounded/filled polygons on Layer 5 for controlled impedance lines.

** Layer 5 has grounded/filled polygons on Layer 6 for controlled impedance lines.

2. Multi Standard Core Module - MSCMOD

The simple and robust architecture of MSCMOD is shown on the block diagram below.



The heart of the board is a Xilinx Virtex-5 family FPGA device.
The PCB can accomodate two types of devices:

- XC5VLX110T-2FF1136C (for MSCMOD board)
- XC5VLX50T-1FF1136C (for MSCMODL board)

The main characteristics of the devices are shown in the table below:

	XC5VLX110T	XC5VLX50T
Array metric	160x54	120x30
Slices	17280	7200
LUT RAM	1120 kBytes	480 kBytes
Block RAM	5.32 MBytes	2.16 MBytes
DSP slices	64	48
GTP Transceivers	16 (8 pairs)	12 (6 pairs)
Clock Management Tiles	8	6

In addition, both types have

- Clock Management Tiles (CMTs) having two Digital Clock Managers (DCM) and a Phase Locked Loop per CMT
- One PCI Express Endpoint Controller
- 4 Tri-mode (10/100/1000)Ethernet Media Access Controller (MAC)
- 2 Internal Configuration Acces Ports (ICAP)
- Core logic can run at 550MHz internal clock speed

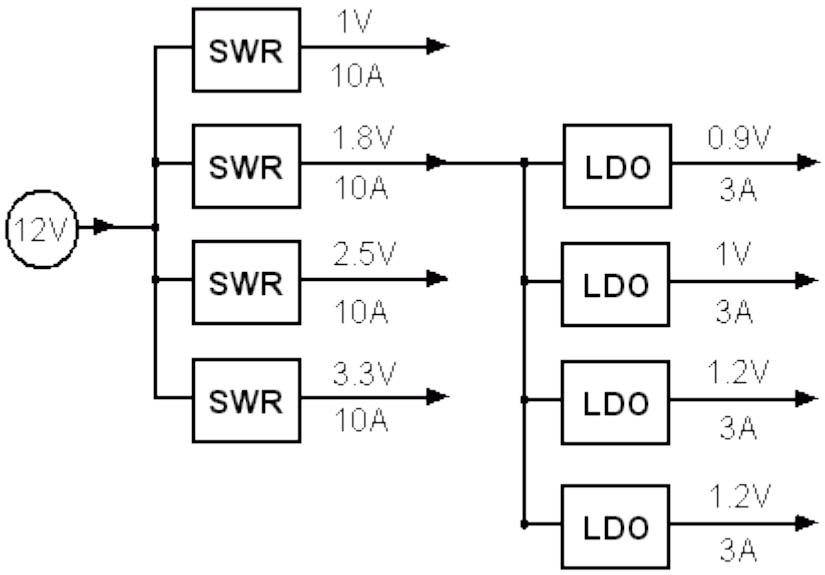
Two MSCMOD models can be produced depending on the insertion of FPGA type as shown below:

Model	FPGA	Ring capacity
MSCMOD	XC5VLX110TCW	4 lanes, ACW 4 lanes (2x12 Gbps)
MSCMODL	XC5VLX50T	CW 2 lanes, ACW 2 lanes (2x6 Gbps)

The following sections detail the rest of the modules's architectual elements.

2.1 Power Supply

The figure below shows the power distribution tree for MSCMOD.
The first stages consist of switching regulator modules (SWR), since on second stages there are low drop-out (LDO) point of load (POL) type regulators.



The signal names, nominal voltages, maximum load current, and designated targets are the following:

Signal name	V	A	Targets	Notes
VCC1	1.0	10	FPGA	Core voltage
VCC1V8	1.8	5	DDR2 RAM	Main supply

	. .	LDO Feed	for DDR2 Ref.
	. .	FPGA I/O	Bank 11,13,15,17,(19,21)
	. .	FLASH	Internal voltage
VCC2V5	1.65	LDO Feed	For MGT LDOs
	. .	FPGA	Auxiliary voltage
	. .	XFP/XAUI	Auxiliary voltage
VCC3V3	3.310	SFPs/XFPs	main power
	. .	FPGA I/O	Bank 20,1,3,0,2,4,(12,5,23,18,6,25)
	. .	Feature Conn.	for I/O std. only
	. .	FLASH/JTAG	I/O voltage
	. .	DDR2	Supply SPD ROM
VCC0V9	0.93	DDR2	Reference voltage
AVCC1	1.03	FPGA MGT	MGT's core voltage
AVCPLL1V2	1.23	FPGA MGT	MGT's PLL supply
VCC5	5 .	XFP aux.	XPF aux. power
VCC1V2	1.222	XFP/XAUI	XFP/XAUI converter Main supply

2.2 Clock sources

There are four clock sources available on MSCMOD for the FPGA cores. The following tables shows their name, nominal frequencies, designated FPGA pins, and the application.

Signal	Source	f [MHz]	FPGA#	Application
REF0CKN	*Ext.	156.25	D4	Ring reference clock,
REF0CKP	.	.	E4	ClockWise (CW), External
REF1CKN	*X1	155.52	AF3	SFP, SDH Telecom. Apps.
REF1CKP	.	.	AF4	.
REF2CKN	*X2	125.00	H3	SFP, Gigabit Ethernet Apps.
REF2CKP	.	.	H4	.
REF3CKN	*X3	156.25	Y3	XFP, 10 G Ethernet App. and
REF3CKP	.	.	Y4	Ring AntiClockWise (ACW)
GCLKN	X4	200.00	L18	System/Global Clock, and
GCLKP	.	.	K17	DDR2 reference clock

* These clock references are routed to MGT clock pins.
Xn designates LVPECL Crystal Oscillators on board.

2.3 Network interfaces

2.3.1 XFI/XAUI conversion for 10Gbps Ethernet (XFP)

CBOARD has two XFP support module for 10 Gigabits Ethernet interfaces. XFI/XAUI conversion allows to feed high speed data at an affordable rate to the FPGA.

Dedicated 156.25 MHz reference clock source is available for FPGA reference and XAUI/XFI converter chip.

The table below lists pinout of FPGA connectivity.

U14 Signals	Function	FPGA#
TRSTN	Reset (active low)	AF11
MDIO	MDIO data	AL10
MDC	MDIO clock	AJ10
CDRLOL	Loss of Lock in CDR	AE11
CMULOL	Loss of Lock in CMU	AH10
TTXON	TX enable	AG11
XRXDP[0]	XAUI RX lane 0	T1
XRXDN[0]		R1
XRXDP[1]	XAUI RX lane 1	N1
XRXDN[1]		P1
XRXDP[2]	XAUI RX lane 2	K1
XRXDN[2]		J1
XRXDP[3]	XAUI RX lane 3	G1
XRXDN[3]		H1
XTXDP[0]	XAUI TX lane 0	U2
XTXDN[0]		T2
XTXDP[1]	XAUI TX lane 1	M2
XTXDN[1]		N2
XTXDP[2]	XAUI TX lane 2	L2
XTXDN[2]		K2
XTXDP[3]	XAUI TX lane 3	F2
XTXDN[3]		G2

* RXPOLARITY attribute for the MGT has to be changed
** TXPOLARITY attribute for the MGT has to be changed

2.3.2 Multi-standard multi-rate interfaces (SFP)

For multistandard applications CBOARD has eight SFP receptacle module routed to this MSC.

Dedicated 155.56 MHz reference clock for SDH and 125.00 MHz source is available for GE applications.

The table below lists pinout of FPGA connectivity.

SFP Signals	Function	FPGA#
MRP[0]	SFP 0 RX lane	AE1
MRN[0]		AF1
MRP[1]	SFP 1 RX lane	AH1
MRN[1]		AG1
MRP[2]	SFP 2 RX lane	W1
MRN[2]		Y1
MRP[3]	SFP 3 RX lane	AB1
MRN[3]		AA1
MTP[0]	SFP 0 TX lane	AD2
MTN[0]		AE2
MTP[1]	SFP 1 TX lane	AJ2
MTN[1]		AH2
MTP[2]	SFP 2 TX lane	V2

MTN[2]		W2
MTP[3]	SFP 3 TX lane	AC2
MTN[3]		AB2

* RXPOLARITY attribute for the MGT has to be changed
** TXPOLARITY attribute for the MGT has to be changed

2.4 Gigabit Ring

The cores on CBOARD communicate each other using Gigabit Ring. Data can be driven clockwise, and anticlockwise to the neighbours.

The table below lists the connectors pins and any associated FPGA connectivity.

Clockwise Signal	FPGA#	Function	Anticlockwise Signal	FPGA#	Function
CTP0	E2	TX lane 0+	ATP0	AK2	TX lane 0+
CTN0	D2	TX lane 0-	ATN0	AL2	TX lane 0-
CTP1	B4	TX lane 1+	ATP1	AN4	TX lane 1+
CTN1	B3	TX lane 1-	ATN1	AN3	TX lane 1-
CTP2	B5	TX lane 2+	ATP2	AN5	TX lane 2+
CTN2	B6	TX lane 2-	ATN2	AN6	TX lane 2-
CTP3	B10	TX lane 3+	ATP3	AN10	TX lane 3+
CTN3	B9	TX lane 3-	ATN3	AN9	TX lane 3-
CRP0	AL1	RX lane 0+	ARP0	D1	RX lane 0+
CRN0	AM1	RX lane 0-	ARN0	C1	RX lane 0-
CRP1	AP3	RX lane 1+	ARP1	A3	RX lane 1+
CRN1	AP2	RX lane 1-	ARN1	A2	RX lane 1-
CRP2	AP6	RX lane 2+	ARP2	A6	RX lane 2+
CRN2	AP7	RX lane 2-	ARN2	A7	RX lane 2-
CRP3	AP9	RX lane 3+	ARP3	A9	RX lane 3+
CRN3	AP8	RX lane 3-	ARN3	A8	RX lane 3-

2.5 DDR2 SODIMM RAM

The MSCMOD board contains a 200-pin, small-outline dual in-line memory module (SODIMM) receptacle (J3) that supports installation of DDR2 SDRAM SODIMMs of 128MB, 256MB, or 512 MB.

Dual-rank SODIMMs may not be supported. Also, the speed grade of -1 of the default FPGA installation limits the DDR2 memory clock support to a range of 200-233MHz (400-466 million transfers per second - double rate).

A 256MB DDR2-667 SODIMM (Micron Semiconductor part number MT4HTF3264HY-667D3) is shipped with MSCMOD - by default.

The SODIMM interface may support customer installation of DDR2-533 and/or DDR2-400 SODIMMs too.

The table below provides a description of the memory interface signals SODIMM connector pin assignments, and the associated FPGA pin assignments.

Signal (Front)	DIMM#	FPGA#	Signal (Back)	DIMM#	FPGA#
VCC0V9	001	-	GND	002	-
GND	003	-	DQ[4]	004	H29
DQ[0]	005	L29	DQ[5]	006	G30
DQ[1]	007	J29	GND	008	-
GND	009	-	DM[0]	010	H30
DQS_N[0]	011	F29	GND	012	-
DQS[0]	013	E29	DQ[6]	014	F30
GND	015	-	DQ[7]	016	G31
DQ[2]	017	P29	GND	018	-
DQ[3]	019	P30	DQ[12]	020	L30
GND	021	-	DQ[13]	022	K31
DQ[8]	023	F31	GND	024	-
DQ[9]	025	E31	DM[1]	026	J31
GND	027	-	GND	028	-
DQS_N[1]	029	N30	CK[0]	030	B32
DQS[1]	031	M31	CK_N[0]	032	A33
GND	033	-	GND	034	-
DQ[10]	035	P31	DQ[14]	036	M30
DQ[11]	037	R31	DQ[15]	038	N29
GND	039	-	GND	040	-
GND	041	-	GND	042	-
DQ[16]	043	B33	DQ[20]	044	C34
DQ[17]	045	C33	DQ[21]	046	D34
GND	047	-	GND	048	-
DQS_N[2]	049	E34	NC/EVENT_N	050	-
DQS[2]	051	F33	DM[2]	052	E33
GND	053	-	GND	054	-
DQ[18]	055	F34	DQ[22]	056	C32
DQ[19]	057	E32	DQ[23]	058	D32
GND	059	-	GND	060	-
DQ[24]	061	H34	DQ[28]	062	G33
DQ[25]	063	H33	DQ[29]	064	G32
GND	065	-	GND	066	-
DM[3]	067	J34	DQS_N[3]	068	K34
NC/RESET_N	069	-	DQS[3]	070	L34
GND	071	-	GND	072	-
DQ[26]	073	K32	DQ[30]	074	J32
DQ[27]	075	L33	DQ[31]	076	K33
GND	077	-	GND	078	-
CKE[0]	079	N32	CKE[1]	080	M32
VCC1V8	081	-	VCC1V8	082	-
NC/CSN[2]	083	-	A[15]	084	R32
BA[2]	085	P32	A[14]	086	R33
VCC1V8	087	-	VCC1V8	088	-
A[12]	089	U31	A[11]	090	T33
A[9]	091	P34	A[7]	092	U32
A[8]	093	V25	A[6]	094	U33
VCC1V8	095	-	VCC1V8	096	-
A[5]	097	W29	A[4]	098	Y28
A[3]	099	R34	A[2]	100	V29

A[1]	101	V24	A[0]	102	AA30
VCC1V8	103	-	VCC1V8	104	-
A[10]	105	W26	BA[1]	106	W31
BA[0]	107	V27	RAS_N	108	AA31
WE_N	109	V28	CS_N[0]	110	Y31
VCC1V8	111	-	VCC1V8	112	-
CAS_N	113	Y29	ODT[0]	114	T34
CS_N[1]	115	AA29	A[13]	116	AB31
VCC1V8	117	-	VCC1V8	118	-
ODT[1]	119	V30	NC/CSN[3]	120	-
GND	121	-	GND	122	-
DQ[32]	123	V32	DQ[36]	124	Y33
DQ[33]	125	V33	DQ[37]	126	Y32
GND	127	-	GND	128	-
DQS_N[4]	129	V34	DM[4]	130	AB32
DQS[4]	131	W34	GND	132	-
GND	133	-	DQ[38]	134	Y34
DQ[34]	135	AA33	DQ[39]	136	AA34
DQ[35]	137	AB33	GND	138	-
GND	139	-	DQ[44]	140	AD32
DQ[40]	141	AC32	DQ[45]	142	AK32
DQ[41]	143	AC33	GND	144	-
GND	145	-	DQS_N[5]	146	AD34
DM[5]	147	AE33	DQS[5]	148	AC34
GND	149	-	GND	150	-
DQ[42]	151	AE32	DQ[46]	152	AF33
DQ[43]	153	AE34	DQ[47]	154	AF34
GND	155	-	GND	156	-
DQ[48]	157	AH34	DQ[52]	158	AM33
DQ[49]	159	AJ34	DQ[53]	160	AK34
GND	161	-	GND	162	-
NC/TEST	163	-	CK[1]	164	AN34
GND	165	-	CK_N[1]	166	AN33
DQS_N[6]	167	AL33	GND	168	-
DQS[6]	169	AL34	DM[6]	170	AN32
GND	171	-	GND	172	-
DQ[50]	173	AK33	DQ[54]	174	AP32
DQ[51]	175	AJ32	DQ[55]	176	AM32
GND	177	-	GND	178	-
DQ[56]	179	AF31	DQ[60]	180	AK31
DQ[57]	181	AG30	DQ[61]	182	AD30
GND	183	-	GND	184	-
DM[7]	185	AF30	DQS_N[7]	186	AH30
GND	187	-	DQS[7]	188	AJ30
DQ[58]	189	AD29	GND	190	-
DQ[59]	191	AE29	DQ[62]	192	AH29
GND	193	-	DQ[63]	194	AF29
SDA	195	AH19	GND	196	-
SCL	197	AF19	SA0	198	(GND)
VCC3V3	199	-	SA1	200	(GND)

2.6 Feature Connector

A TDM bus is used to carry OAM messages and timing reference.

The table below shows the clock/data pin assignment for OAM TDM.

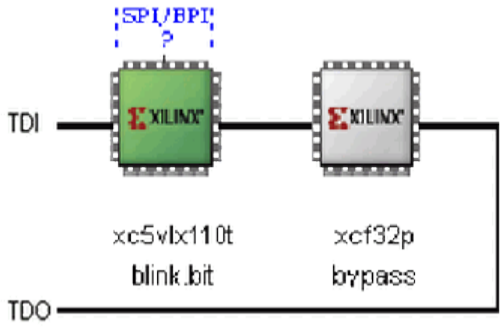
Signals	Function	FPGA#
TCL	TDM Clock	E13
TDA	TDM Data	F13

2.7 FPGA Programming

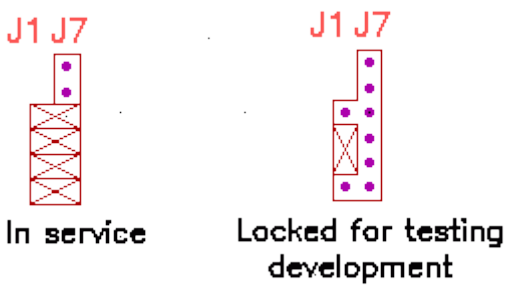
Three configuration methods are available on MSCMOD to upload (program) the FPGA core.

2.7.1 Programming through JTAG

The FPGA core can be loaded directly through the JTAG port (designated as J7 on-board) as shown in the figure below

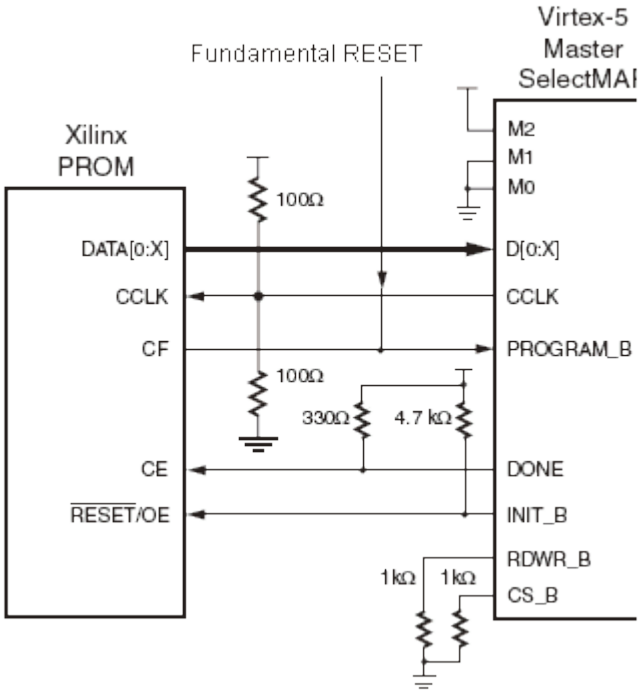


The module can be chained into board level JTAG using jumpers (J1,J7) as shown in the figure below.



2.7.2 Programming from FLASH

From the Platform FLASH (designated as U11), the FPGA can be loaded automatically.
If J4 jumper is open - it happens one time during the power-up.
If J4 is closed, every fundamental reset causes reconfiguration of the FPGA from the Platform FLASH.
The FLASH itself has to be burned through the JTAG with a valid configuration stream.



2.7.3 Partial reconfiguration

If the Platform FLASH contains the proper core implementing a PCI Express endpoint, and a controller core for ICAP (Internal Configuration Access Port) - this RESIDENT core allows the Partial reconfiguration of the FPGA.
TRANSIENT cores can be loaded that way.

J6 jumper controls HSWAPEN.

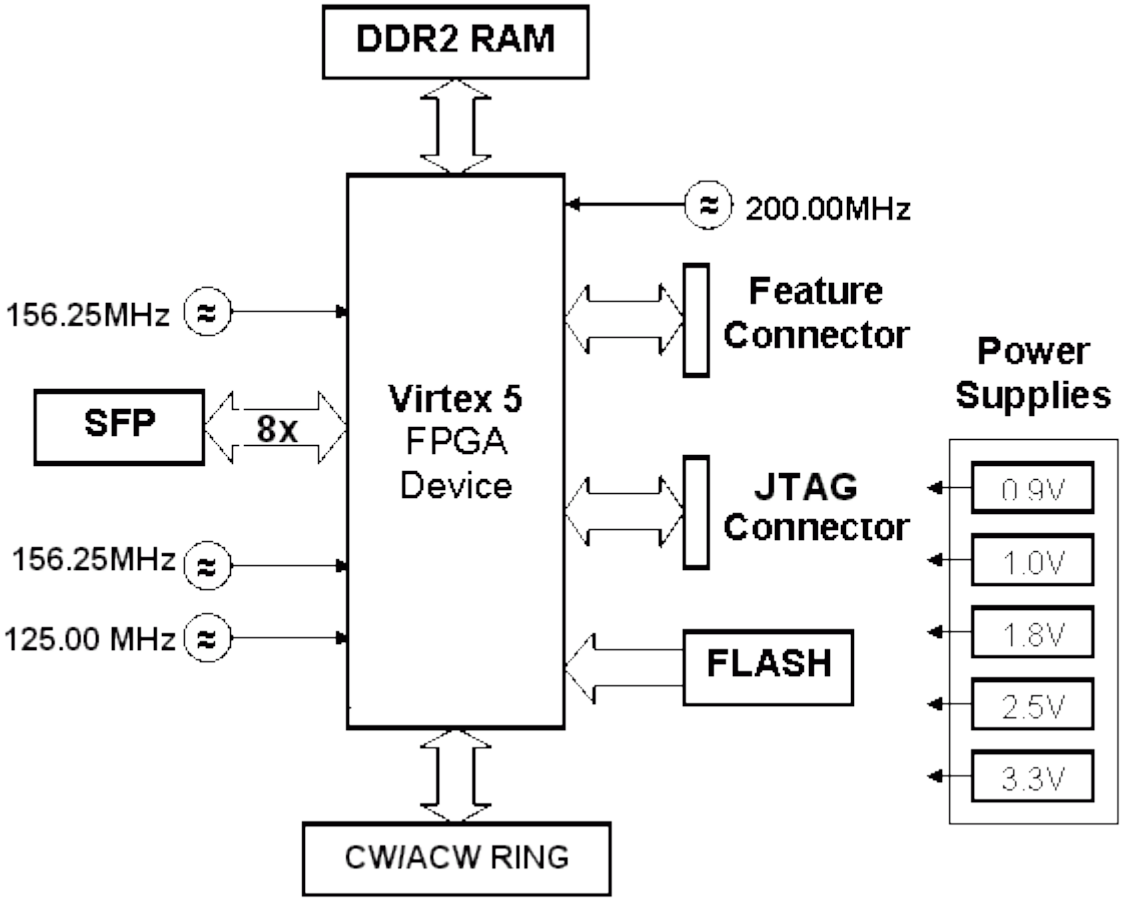
2.8 Status LEDs

There are two status LEDs assigned to a MSC module.
One red colored MFAULT (Module Fault or alarms) and one green colored MACT (Module Activity). The table below summarizes the assignment:

Signal	LED	FPGA#
MACT	Green	H15
MFAULT	Red	G15

3. Gigabit Ethernet Switch Module - SWCMOD

The simple and robust architecture of SWCMOD is shown on the block diagram below.



The heart of the board is a Xilinx Virtex-5 family FPGA device.
The PCB can accomodate two types of devices:

- XC5VLX110T-2FF1136C (for SWCMOD board)
- XC5VLX50T-1FF1136C (for SWCMODL board)

The main characteristics of the devices are shown in the table below:

	XC5VLX110T	XC5VLX50T
Array metric	160x54	120x30
Slices	17280	7200
LUT RAM	1120 kBytes	480 kBytes
Block RAM	5.32 MBytes	3.16 MBytes
DSP slices	64	48
GTP Transceivers	16 (8 pairs)	12 (6 pairs)
Clock Management Tiles	8	6

In addition, both types have

- Clock Management Tiles (CMTs) having two Digital Clock Managers (DCM) and a Phase Locked Loop per CMT
- One PCI Express Endpoint Controller
- 4 Tri-mode (10/100/1000)Ethernet Media Access Controller (MAC)
- 2 Internal Configuration Acces Ports (ICAP)
- Core logic can run at 550MHz internal clock speed

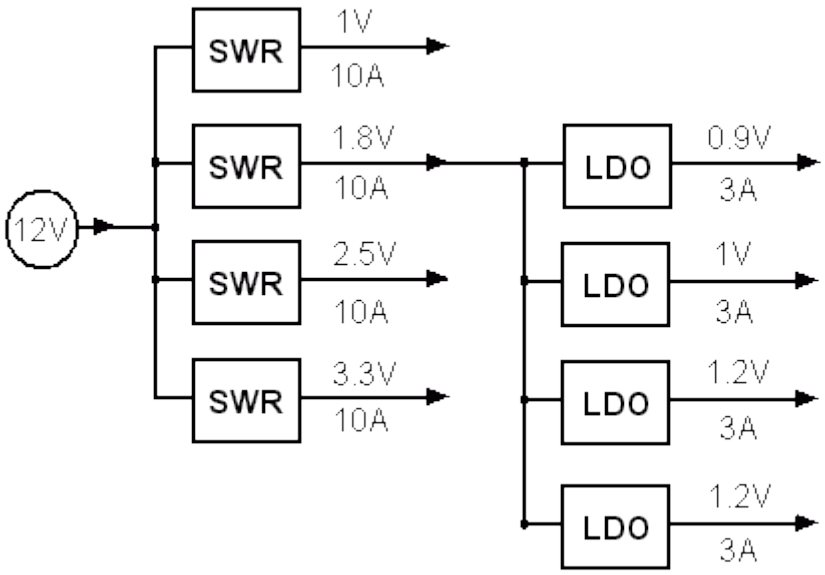
Two SWCMOD models can be produced depending on the insertion of FPGA type as shown below:

Model	FPGA	Ring capacity
SWCMOD	XC5VLX110TCW	4 lanes, ACW 4 lanes (2x12 Gbps)
SWCMODL	XC5VLX50T	CW 2 lanes, ACW 2 lanes (2x6 Gbps)

The following sections detail the rest of the modules's architectual elements.

3.1 Power Supply

The figure below shows the power distribution tree for SWCMOD.
The first stages consist of switching regulator modules (SWR), since on second stages there are low drop-out (LDO) point of load (POL) type regulators.



The signal names, nominal voltages, maximum load current, and designated targets are the following:

Signal name	V	A	Targets	Notes
VCC1	1.0	10	FPGA	Core voltage
VCC1V8	1.8	5	DDR2 RAM	Main supply

	. .	LDO Feed	for DDR2 Ref.
	. .	FPGA I/O	Bank 11,13,15,17,(19,21)
	. .	FLASH	Internal voltage
VCC2V5	1.65	LDO Feed	For MGT LDOs
	. .	FPGA	Auxiliary voltage
	. .	XFP/XAUI	Auxiliary voltage
VCC3V3	3.310	SFPs/XFPs	main power
	. .	FPGA I/O	Bank 20,1,3,0,2,4,(12,5,23,18,6,25)
	. .	Feature Conn.	for I/O std. only
	. .	FLASH/JTAG	I/O voltage
	. .	DDR2	Supply SPD ROM
VCC0V9	0.93	DDR2	Reference voltage
AVCC1	1.03	FPGA MGT	MGT's core voltage
AVCPLL1V2	1.23	FPGA MGT	MGT's PLL supply
VCC5	5 .	XFP aux.	XPF aux. power
VCC1V2	1.222	XFP/XAUI	XFP/XAUI converter Main supply

3.2 Clock sources

There are four clock sources available on SWCMOD for the FPGA cores. The following tables shows their name, nominal frequencies, designated FPGA pins, and the application.

Signal	Source	f [MHz]	FPGA#	Application
REF1CKN	*X1	156.25	AF3	Ring ClockWise (CW)
REF1CKP	.	.	AF4	.
REF2CKN	*X2	125.00	H3	SFP, Gigabit Ethernet Apps.
REF2CKP	.	.	H4	.
REF3CKN	*X3	156.25	Y3	Ring AntiClockWise (AC)
REF3CKP	.	.	Y4	.
GCLKN	X4	200.00	L18	System/Global Clock, and
GCLKP	.	.	K17	DDR2 reference clock

* These clock references are routed to MGT clock pins.
Xn designates LVPECL Crystal Oscillators on board.

3.3 Network Interfaces

CBOARD has eight SFP support module for Gigabits Ethernet interfaces. The module drives the SFP lanes directly.

Dedicated 125.00 MHz reference clock source is available for FPGA reference.

The table below lists pinout of SFP's FPGA connectivity.

Signals	Function	FPGA#
GRP[0]	SFP 0 RX lane	AE1
GRN[0]		AF1
GTP[0]	SFP 0 TX lane	AD2

GTN[0]		AE2
GRP[1]	SFP 1 RX lane	AH1
GRN[1]		AG1
GTP[1]	SFP 1 TX lane	AJ2
GTN[1]		AH2
GRP[2]	SFP 2 RX lane	W1
GRN[2]		Y1
GTP[2]	SFP 2 TX lane	V2
GTN[2]		W2
GRP[3]	SFP 3 RX lane	AB1
GRN[3]		AA1
GTP[3]	SFP 3 TX lane	AC2
GTN[3]		AB2
GRP[4]	SFP 4 RX lane	N1
GRN[4]		P1
GTP[4]	SFP 4 TX lane	M2
GTN[4]		N2
GRP[5]	SFP 5 RX lane	T1
GRN[5]		R1
GTP[5]	SFP 5 TX lane	U2
GTN[5]		T2
GRP[6]	SFP 6 RX lane	G1
GRN[6]		H1
GTP[6]	SFP 6 TX lane	F2
GTN[6]		G2
GRP[7]	SFP 7 RX lane	K1
GRN[7]		J1
GTP[7]	SFP 7 TX lane	L2
GTN[7]		K2

* RXPOLARITY attribute for the MGT has to be changed
** TXPOLARITY attribute for the MGT has to be changed

3.4 Gigabit Ring

The cores on CBOARD communicate each other using Gigabit Ring. Data can be driven clockwise, and anticlockwise to the neighbours.

The table below lists the connectors pins and any associated FPGA connectivity.

Clockwise Signal	FPGA#	Function	Anticlockwise Signal	FPGA#	Function
CTP0	E2	TX lane 0+	ATP0	AK2	TX lane 0+
CTN0	D2	TX lane 0-	ATN0	AL2	TX lane 0-
CTP1	B4	TX lane 1+	ATP1	AN4	TX lane 1+
CTN1	B3	TX lane 1-	ATN1	AN3	TX lane 1-
CTP2	B5	TX lane 2+	ATP2	AN5	TX lane 2+
CTN2	B6	TX lane 2-	ATN2	AN6	TX lane 2-
CTP3	B10	TX lane 3+	ATP3	AN10	TX lane 3+
CTN3	B9	TX lane 3-	ATN3	AN9	TX lane 3-
CRP0	AL1	RX lane 0+	ARP0	D1	RX lane 0+

CRN0	AM1	RX lane 0-	ARN0	C1	RX lane 0-
CRP1	AP3	RX lane 1+	ARP1	A3	RX lane 1+
CRN1	AP2	RX lane 1-	ARN1	A2	RX lane 1-
CRP2	AP6	RX lane 2+	ARP2	A6	RX lane 2+
CRN2	AP7	RX lane 2-	ARN2	A7	RX lane 2-
CRP3	AP9	RX lane 3+	ARP3	A9	RX lane 3+
CRN3	AP8	RX lane 3-	ARN3	A8	RX lane 3-

3.5 DDR2 SODIMM RAM

The SWCMOD board contains a 200-pin, small-outline dual in-line memory module (SODIMM) receptacle (J3) that supports installation of DDR2 SDRAM SODIMMs of 128MB, 256MB, or 512 MB.

Dual-rank SODIMMs may not be supported. Also, the speed grade of -1 of the default FPGA installation limits the DDR2 memory clock support to a range of 200-233MHz (400-466 million transfers per second - double rate).

A 256MB DDR2-667 SODIMM (Micron Semiconductor part number MT4HTF3264HY-667D3) is shipped with SWCMOD - by default.

The SODIMM interface may support customer installation of DDR2-533 and/or DDR2-400 SODIMMs too.

The table below provides a description of the memory interface signals SODIMM connector pin assignments, and the associated FPGA pin assignments.

Signal (Front)	DIMM#	FPGA#	Signal (Back)	DIMM#	FPGA#
VCC0V9	001	-	GND	002	-
GND	003	-	DQ[4]	004	H29
DQ[0]	005	L29	DQ[5]	006	G30
DQ[1]	007	J29	GND	008	-
GND	009	-	DM[0]	010	H30
DQS_N[0]	011	F29	GND	012	-
DQS[0]	013	E29	DQ[6]	014	F30
GND	015	-	DQ[7]	016	G31
DQ[2]	017	P29	GND	018	-
DQ[3]	019	P30	DQ[12]	020	L30
GND	021	-	DQ[13]	022	K31
DQ[8]	023	F31	GND	024	-
DQ[9]	025	E31	DM[1]	026	J31
GND	027	-	GND	028	-
DQS_N[1]	029	N30	CK[0]	030	B32
DQS[1]	031	M31	CK_N[0]	032	A33
GND	033	-	GND	034	-
DQ[10]	035	P31	DQ[14]	036	M30
DQ[11]	037	R31	DQ[15]	038	N29
GND	039	-	GND	040	-
GND	041	-	GND	042	-
DQ[16]	043	B33	DQ[20]	044	C34
DQ[17]	045	C33	DQ[21]	046	D34
GND	047	-	GND	048	-

DQS_N[2]	049	E34	NC/EVENT_N	050	-
DQS[2]	051	F33	DM[2]	052	E33
GND	053	-	GND	054	-
DQ[18]	055	F34	DQ[22]	056	C32
DQ[19]	057	E32	DQ[23]	058	D32
GND	059	-	GND	060	-
DQ[24]	061	H34	DQ[28]	062	G33
DQ[25]	063	H33	DQ[29]	064	G32
GND	065	-	GND	066	-
DM[3]	067	J34	DQS_N[3]	068	K34
NC/RESET_N	069	-	DQS[3]	070	L34
GND	071	-	GND	072	-
DQ[26]	073	K32	DQ[30]	074	J32
DQ[27]	075	L33	DQ[31]	076	K33
GND	077	-	GND	078	-
CKE[0]	079	N32	CKE[1]	080	M32
VCC1V8	081	-	VCC1V8	082	-
NC/CSN[2]	083	-	A[15]	084	R32
BA[2]	085	P32	A[14]	086	R33
VCC1V8	087	-	VCC1V8	088	-
A[12]	089	U31	A[11]	090	T33
A[9]	091	P34	A[7]	092	U32
A[8]	093	V25	A[6]	094	U33
VCC1V8	095	-	VCC1V8	096	-
A[5]	097	W29	A[4]	098	Y28
A[3]	099	R34	A[2]	100	V29
A[1]	101	V24	A[0]	102	AA30
VCC1V8	103	-	VCC1V8	104	-
A[10]	105	W26	BA[1]	106	W31
BA[0]	107	V27	RAS_N	108	AA31
WE_N	109	V28	CS_N[0]	110	Y31
VCC1V8	111	-	VCC1V8	112	-
CAS_N	113	Y29	ODT[0]	114	T34
CS_N[1]	115	AA29	A[13]	116	AB31
VCC1V8	117	-	VCC1V8	118	-
ODT[1]	119	V30	NC/CSN[3]	120	-
GND	121	-	GND	122	-
DQ[32]	123	V32	DQ[36]	124	Y33
DQ[33]	125	V33	DQ[37]	126	Y32
GND	127	-	GND	128	-
DQS_N[4]	129	V34	DM[4]	130	AB32
DQS[4]	131	W34	GND	132	-
GND	133	-	DQ[38]	134	Y34
DQ[34]	135	AA33	DQ[39]	136	AA34
DQ[35]	137	AB33	GND	138	-
GND	139	-	DQ[44]	140	AD32
DQ[40]	141	AC32	DQ[45]	142	AK32
DQ[41]	143	AC33	GND	144	-
GND	145	-	DQS_N[5]	146	AD34
DM[5]	147	AE33	DQS[5]	148	AC34
GND	149	-	GND	150	-
DQ[42]	151	AE32	DQ[46]	152	AF33
DQ[43]	153	AE34	DQ[47]	154	AF34
GND	155	-	GND	156	-

DQ[48]	157	AH34	DQ[52]	158	AM33
DQ[49]	159	AJ34	DQ[53]	160	AK34
GND	161	-	GND	162	-
NC/TEST	163	-	CK[1]	164	AN34
GND	165	-	CK_N[1]	166	AN33
DQS_N[6]	167	AL33	GND	168	-
DQS[6]	169	AL34	DM[6]	170	AN32
GND	171	-	GND	172	-
DQ[50]	173	AK33	DQ[54]	174	AP32
DQ[51]	175	AJ32	DQ[55]	176	AM32
GND	177	-	GND	178	-
DQ[56]	179	AF31	DQ[60]	180	AK31
DQ[57]	181	AG30	DQ[61]	182	AD30
GND	183	-	GND	184	-
DM[7]	185	AF30	DQS_N[7]	186	AH30
GND	187	-	DQS[7]	188	AJ30
DQ[58]	189	AD29	GND	190	-
DQ[59]	191	AE29	DQ[62]	192	AH29
GND	193	-	DQ[63]	194	AF29
SDA	195	AH19	GND	196	-
SCL	197	AF19	SA0	198	(GND)
VCC3V3	199	-	SA1	200	(GND)

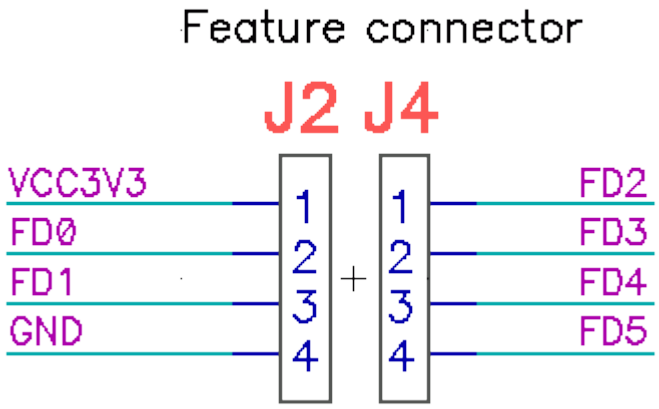
3.6 Feature Connector

A TDM bus is used to carry OAM messages and timing reference.

The table below shows the clock/data pin assignment for OAM TDM.

Signals	Function	FPGA#
TCL	TDM Clock	E13
TDA	TDM Data	F13

J2, and J4 headers support auxiliary functions, such as legacy PCM interfaces.



The table below shows the pin assignment for legacy TDM.

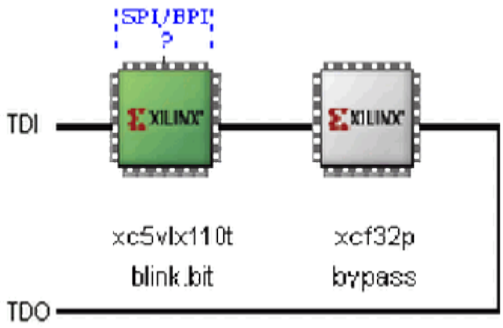
Signals	Function	FPGA#
FD0	Feature data 0	AG11
FD1	Feature data 1	AJ10
FD2	Feature data 2	AL10
FD3	Feature data 3	AH10
FD4	Feature data 4	AE11
FD5	Feature data 5	AF11

3.7 FPGA Programming

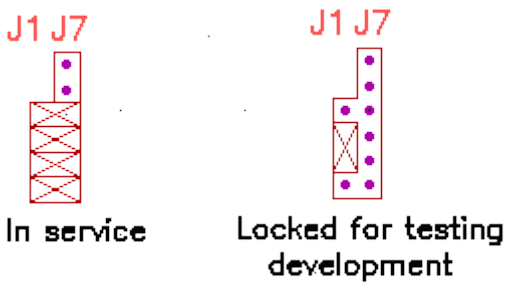
Three configuration methods are available on SWCMOD to upload (program) the FPGA core.

3.7.1 Programming through JTAG

The FPGA core can be loaded directly through the JTAG port (designated as J7 on-board) as shown in the figure below



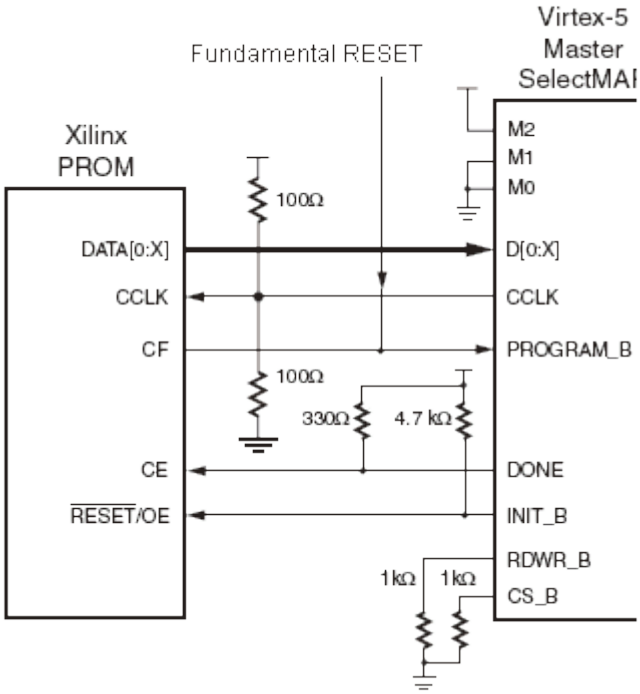
The module can be chained into board level JTAG using jumpers (J1,J7) as shown in the figure below.



3.7.2 Programming from FLASH

From the Platform FLASH (designated as U11), the FPGA can be loaded automatically.
If J4 jumper is open - it happens one time during the power-up.
If J4 is closed, every fundamental reset causes reconfiguration of the FPGA from the Platform

FLASH.
The FLASH itself has to be burned through the JTAG with a valid configuration stream.



3.7.3 Partial reconfiguration

If the Platform FLASH contains the proper core implementing a PCI Express endpoint, and a controller core for ICAP (Internal Configuration Access Port) - this RESIDENT core allows the Partial reconfiguration of the FPGA.
TRANSIENT cores can be loaded that way.

J6 jumper controls HSWAPEN.

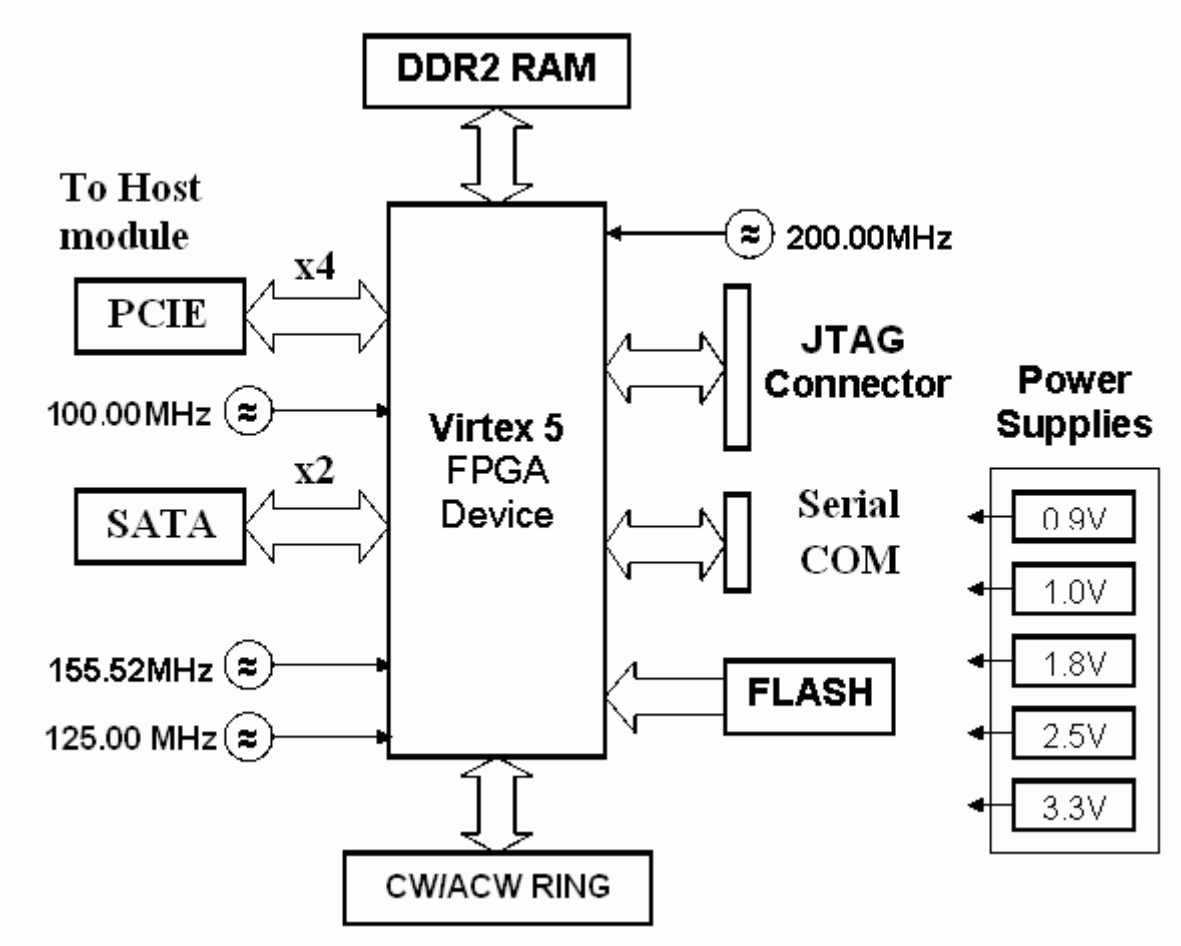
3.8 Status LEDs

There are two status LEDs assigned to a SWC module.
One red colored MFAULT (Module Fault or alarms) and one green colored MACT (Module Activity). The table below summarizes the assignment:

Signal	LED	FPGA#
MACT	Green	H15
MFAULT	Red	G15

4. Management Host Core Module - MHCMOD

The simple and robust architecture of MHCMOD is shown on the block diagram below.



The heart of the board is a Xilinx Virtex-5 family FPGA device.
The PCB can accomodate two types of devices:

- XC5VLX110T-2FF1136C (for MHCMOD board)
- XC5VLX50T-1FF1136C (for MHCMODL board)

The main characteristics of the devices are shown in the table below:

	XC5VLX110T	XC5VLX50T
Array metric	160x54	120x30
Slices	17280	7200
LUT RAM	1120 kBytes	480 kBytes
Block RAM	5.32 MBytes	2.16 MBytes
DSP slices	64	48
GTP Transceivers	16 (8 pairs)	12 (6 pairs)
Clock Management Tiles	8	6

In addition, both types have

- Clock Management Tiles (CMTs) having two Digital Clock Managers (DCM) and a Phase Locked Loop per CMT
- One PCI Express Endpoint Controller
- 4 Tri-mode (10/100/1000)Ethernet Media Access Controller (MAC)
- 2 Internal Configuration Acces Ports (ICAP)
- Core logic can run at 550MHz internal clock speed

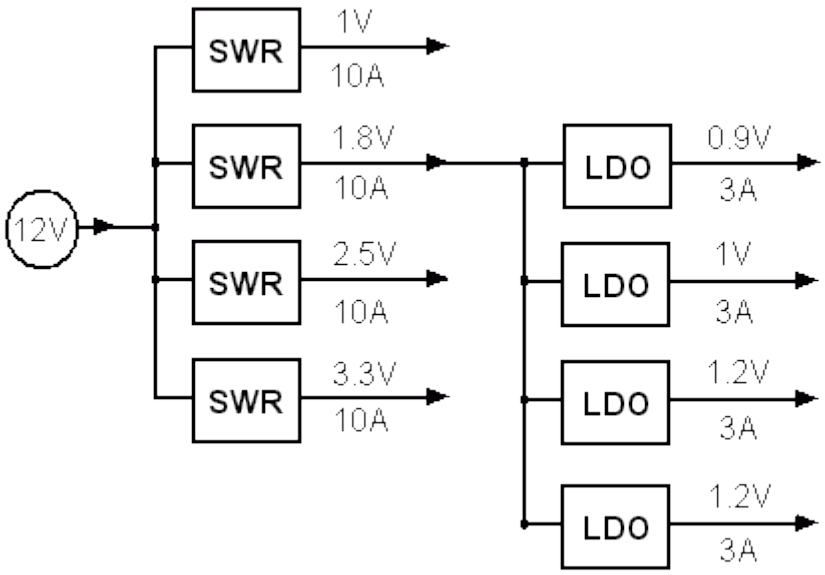
Two MHCMOD models can be produced depending on the insertion of FPGA type as shown below:

Model	FPGA	Ring capacity
MHCMOD	XC5VLX110TCW	4 lanes, ACW 4 lanes (2x12 Gbps)
MHCMODLX	C5VLX50T	CW 2 lanes, ACW 2 lanes (2x6 Gbps)

The following sections detail the rest of the modules's architectual elements.

4.1 Power Supply

The figure below shows the power distribution tree for MHCMOD.
The first stages consist of switching regulator modules (SWR), since on second stages there are low drop-out (LDO) point of load (POL) type regulators.



The signal names, nominal voltages, maximum load current, and designated targets are the following:

Signal name	V	A	Targets	Notes
VCC1	1.0	10	FPGA	Core voltage
VCC1V8	1.8	5	DDR2 RAM	Main supply

	. .	LDO Feed	for DDR2 Ref.
	. .	FPGA I/O	Bank 11,13,15,17,(19,21)
	. .	FLASH	Internal voltage
VCC2V5	1.65	LDO Feed	For MGT LDOs
	. .	FPGA	Auxiliary voltage
	. .	XFP/XAUI	Auxiliary voltage
VCC3V3	3.310	SFPs/XFPs	main power
	. .	FPGA I/O	Bank 20,1,3,0,2,4,(12,5,23,18,6,25)
	. .	Feature Conn.	for I/O std. only
	. .	FLASH/JTAG	I/O voltage
	. .	DDR2	Supply SPD ROM
VCC0V9	0.93	DDR2	Reference voltage
AVCC1	1.03	FPGA MGT	MGT's core voltage
AVCPLL1V2	1.23	FPGA MGT	MGT's PLL supply
VCC5	5 .	XFP aux.	XPF aux. power
VCC1V2	1.222	XFP/XAUI	XFP/XAUI converter Main supply

4.2 Clock sources

There are four clock sources available on MHCMOD for the FPGA cores. The following tables shows their name, nominal frequencies, designated FPGA pins, and the application.

Signal	Source	f [MHz]	FPGA#	Application
REF0CKN	*Ext.	156.25	D4	Ring reference clock,
REF0CKP	.	.	E4	ClockWise (CW), External
REF2CKN	*X2	156.25	H3	And ACW
REF2CKP	.	.	H4	.
REF3CKN	*X3	200.00	Y3	SATA HDD
REF3CKP	.	.	Y4	.
GCLKN	X4	200.00	L18	System/Global Clock, and
GCLKP	.	.	K17	DDR2 reference clock

* These clock references are routed to MGT clock pins.
Xn designates LVPECL Crystal Oscillators on board.

4.3 PCI Express x4 endpoint

The PCI Express endpoint connector (routed to U3 host module) allows an FPGA design to support x1, and x4 gigabit lanes to communicate with the host, at the speed of 2.5 Gbps of each.

The table below lists the connectors pins and any associated FPGA connectivity.

Signal (P1)	Side A	FPGA#	Signal (P2)	Side B	FPGA#
PRESENT_N	A1	-	+12 VOLTS	B1	To PWR
+12 VOLTS	A2	To PWR	+12 VOLTS	B2	To PWR
+12 VOLTS	A3	To PWR	+12 VOLTS	B3	To PWR
GND	A4	-	GND	B4	-
JTAG_TCK	A5	-	SMCLK	B5	-
JTAG_TDI	A6	-	SMDAT	B6	-

JTAG_TDO	A7	-	GND	B7	-
JTAG_TMS	A8	-	+3.3 VOLTS	B8	-
+3.3 VOLTS	A9	-	JTAG_TRST_N	B9	-
+3.3 VOLTS	A10	-	+3.3 VAUX	B10	-
PXPERST	A11	-	PCIE_WAKE_N	B11	-
KEY	KEY	KEY	KEY	KEY	KEY
GND	A12	-	RESERVED	B12	-
PXCLKP	A13	Y4	GND	B13	-
PXCLKN	A14	Y3	PETP0	B14	W1
GND	A15	-	PETN0	B15	Y1
PERP0	A16	V2	GND	B16	-
PERN0	A17	W2	PRESENT_N	B17	-
GND	A18	-	GND	B18	-
RESERVED	A19	-	PETP1	B19	AA1 **
GND	A20	-	PETN1	B20	AB1
PERP1	A21	AB2 *	GND	B21	-
PERN1	A22	AC2	GND	B22	-
GND	A23	-	PETP2	B23	AE1
GND	A24	-	PETN2	B24	AF1
PERP2	A25	AD2	GND	B25	-
PERN2	A26	AE2	GND	B26	-
GND	A27	-	PETP3	B27	AG1 **
GND	A28	-	PETN3	B28	AH1
PERP3	A29	AH2 *	GND	B29	-
PERN3	A30	AJ2	---	B30	-
GND	A31	-	PRESENT4_N	B31	To J2

* RXPOLARITY attribute for the MGT has to be changed
** TXPOLARITY attribute for the MGT has to be changed

Although the PCI identification codes are FPGA core dependeant, defaults are the following:

```
Vendor ID........ 15C6 ..... Technical University of Budapest
Device ID........ CB0D ..... CBOARD Managament Host Core (MHC)
Revision ID......    1 ..... Rev. 1. (SGA10GD)
Base Class.......   02 ..... Network controller
Sub-Class........   80 ..... Other network controller
Interface........    0 ..... Base model, XC5VLX110T
Interface........    1 ..... Lite model, XC5VLX50T
```

4.4 Gigabit Ring

The cores on CBOARD communicate each other using Gigabit Ring. Data can be driven clockwise, and anticlockwise to the neighbours.

The table below lists the connectors pins and any associated FPGA connectivity.

Clockwise Signal	FPGA#	Function	Anticlockwise Signal	FPGA#	Function
CTP0	E2	TX lane 0+	ATP0	AK2	TX lane 0+
CTN0	D2	TX lane 0-	ATN0	AL2	TX lane 0-
CTP1	B4	TX lane 1+	ATP1	AN4	TX lane 1+
CTN1	B3	TX lane 1-	ATN1	AN3	TX lane 1-
CTP2	B5	TX lane 2+	ATP2	AN5	TX lane 2+

CTN2	B6	TX lane 2-	ATN2	AN6	TX lane 2-
CTP3	B10	TX lane 3+	ATP3	AN10	TX lane 3+
CTN3	B9	TX lane 3-	ATN3	AN9	TX lane 3-
CRP0	AL1	RX lane 0+	ARP0	D1	RX lane 0+
CRN0	AM1	RX lane 0-	ARN0	C1	RX lane 0-
CRP1	AP3	RX lane 1+	ARP1	A3	RX lane 1+
CRN1	AP2	RX lane 1-	ARN1	A2	RX lane 1-
CRP2	AP6	RX lane 2+	ARP2	A6	RX lane 2+
CRN2	AP7	RX lane 2-	ARN2	A7	RX lane 2-
CRP3	AP9	RX lane 3+	ARP3	A9	RX lane 3+
CRN3	AP8	RX lane 3-	ARN3	A8	RX lane 3-

4.5 DDR2 SODIMM RAM

The MHCMOD board contains a 200-pin, small-outline dual in-line memory module (SODIMM) receptacle (J3) that supports installation of DDR2 SDRAM SODIMMs of 128MB, 256MB, or 512 MB.

Dual-rank SODIMMs may not be supported. Also, the speed grade of -1 of the default FPGA installation limits the DDR2 memory clock support to a range of 200-233MHz (400-466 million transfers per second - double rate).

A 256MB DDR2-667 SODIMM (Micron Semiconductor part number MT4HTF3264HY-667D3) is shipped with MHCMOD - by default.

The SODIMM interface may support customer installation of DDR2-533 and/or DDR2-400 SODIMMs too.

The table below provides a description of the memory interface signals SODIMM connector pin assignments, and the associated FPGA pin assignments.

Signal (Front)	DIMM#	FPGA#	Signal (Back)	DIMM#	FPGA#
VCC0V9	001	-	GND	002	-
GND	003	-	DQ[4]	004	H29
DQ[0]	005	L29	DQ[5]	006	G30
DQ[1]	007	J29	GND	008	-
GND	009	-	DM[0]	010	H30
DQS_N[0]	011	F29	GND	012	-
DQS[0]	013	E29	DQ[6]	014	F30
GND	015	-	DQ[7]	016	G31
DQ[2]	017	P29	GND	018	-
DQ[3]	019	P30	DQ[12]	020	L30
GND	021	-	DQ[13]	022	K31
DQ[8]	023	F31	GND	024	-
DQ[9]	025	E31	DM[1]	026	J31
GND	027	-	GND	028	-
DQS_N[1]	029	N30	CK[0]	030	B32
DQS[1]	031	M31	CK_N[0]	032	A33
GND	033	-	GND	034	-
DQ[10]	035	P31	DQ[14]	036	M30
DQ[11]	037	R31	DQ[15]	038	N29
GND	039	-	GND	040	-

GND	041	-	GND	042	-
DQ[16]	043	B33	DQ[20]	044	C34
DQ[17]	045	C33	DQ[21]	046	D34
GND	047	-	GND	048	-
DQS_N[2]	049	E34	NC/EVENT_N	050	-
DQS[2]	051	F33	DM[2]	052	E33
GND	053	-	GND	054	-
DQ[18]	055	F34	DQ[22]	056	C32
DQ[19]	057	E32	DQ[23]	058	D32
GND	059	-	GND	060	-
DQ[24]	061	H34	DQ[28]	062	G33
DQ[25]	063	H33	DQ[29]	064	G32
GND	065	-	GND	066	-
DM[3]	067	J34	DQS_N[3]	068	K34
NC/RESET_N	069	-	DQS[3]	070	L34
GND	071	-	GND	072	-
DQ[26]	073	K32	DQ[30]	074	J32
DQ[27]	075	L33	DQ[31]	076	K33
GND	077	-	GND	078	-
CKE[0]	079	N32	CKE[1]	080	M32
VCC1V8	081	-	VCC1V8	082	-
NC/CSN[2]	083	-	A[15]	084	R32
BA[2]	085	P32	A[14]	086	R33
VCC1V8	087	-	VCC1V8	088	-
A[12]	089	U31	A[11]	090	T33
A[9]	091	P34	A[7]	092	U32
A[8]	093	V25	A[6]	094	U33
VCC1V8	095	-	VCC1V8	096	-
A[5]	097	W29	A[4]	098	Y28
A[3]	099	R34	A[2]	100	V29
A[1]	101	V24	A[0]	102	AA30
VCC1V8	103	-	VCC1V8	104	-
A[10]	105	W26	BA[1]	106	W31
BA[0]	107	V27	RAS_N	108	AA31
WE_N	109	V28	CS_N[0]	110	Y31
VCC1V8	111	-	VCC1V8	112	-
CAS_N	113	Y29	ODT[0]	114	T34
CS_N[1]	115	AA29	A[13]	116	AB31
VCC1V8	117	-	VCC1V8	118	-
ODT[1]	119	V30	NC/CSN[3]	120	-
GND	121	-	GND	122	-
DQ[32]	123	V32	DQ[36]	124	Y33
DQ[33]	125	V33	DQ[37]	126	Y32
GND	127	-	GND	128	-
DQS_N[4]	129	V34	DM[4]	130	AB32
DQS[4]	131	W34	GND	132	-
GND	133	-	DQ[38]	134	Y34
DQ[34]	135	AA33	DQ[39]	136	AA34
DQ[35]	137	AB33	GND	138	-
GND	139	-	DQ[44]	140	AD32
DQ[40]	141	AC32	DQ[45]	142	AK32
DQ[41]	143	AC33	GND	144	-
GND	145	-	DQS_N[5]	146	AD34
DM[5]	147	AE33	DQS[5]	148	AC34

GND	149	-	GND	150	-
DQ[42]	151	AE32	DQ[46]	152	AF33
DQ[43]	153	AE34	DQ[47]	154	AF34
GND	155	-	GND	156	-
DQ[48]	157	AH34	DQ[52]	158	AM33
DQ[49]	159	AJ34	DQ[53]	160	AK34
GND	161	-	GND	162	-
NC/TEST	163	-	CK[1]	164	AN34
GND	165	-	CK_N[1]	166	AN33
DQS_N[6]	167	AL33	GND	168	-
DQS[6]	169	AL34	DM[6]	170	AN32
GND	171	-	GND	172	-
DQ[50]	173	AK33	DQ[54]	174	AP32
DQ[51]	175	AJ32	DQ[55]	176	AM32
GND	177	-	GND	178	-
DQ[56]	179	AF31	DQ[60]	180	AK31
DQ[57]	181	AG30	DQ[61]	182	AD30
GND	183	-	GND	184	-
DM[7]	185	AF30	DQS_N[7]	186	AH30
GND	187	-	DQS[7]	188	AJ30
DQ[58]	189	AD29	GND	190	-
DQ[59]	191	AE29	DQ[62]	192	AH29
GND	193	-	DQ[63]	194	AF29
SDA	195	AH19	GND	196	-
SCL	197	AF19	SA0	198	(GND)
VCC3V3	199	-	SA1	200	(GND)

4.6 Serial communication lines

4.6.1 Console port (P1)

A serial communicaton port is attached to MHC allowing direct console access through a DB9 connector.

The table below shows the pin assignment for the console port.

Signals	DB9 pin	FPGA#
CDCD in	1	AG11
CRXD in	2	AE11
CTXD out	3	AJ10
CDTR out	4	AN12
CDSR in	6	AH10
CRTS out	7	AF11
CCTS in	8	AL10
CRI in	9	AP12

4.6.2 SuperIO COM2

In case of on board control by a host module, the second serial port of the Superio chip can be used. The signal routing:

Signals	SuperIO #	FPGA#
SCD out	84	H23
SRXD out	82	K22
STXD in	83	G23
SDTR in	81	J22
SDSR out	79	G22
SRTS in	80	H22
SCTS out	78	K21
SRI out	85	K23

4.6.3 Module control

SFP and XFP network interface modules can be controlled using a set of microcontrollers designated from "A" to "J", using a serial communication bus. The host sends commands to a designated target using **MCMD** signal. The addressed controller returns the results to the **MRES** bus. All others are tri-stated.

Signals	FPGA#
MCMD out	B12
MRES in	A13

A TDM bus is used to carry OAM messages and timing reference. Modules "K" to "M" are mastered by this "N" core.

The table below shows the clock/data pin assignment for OAM TDM.

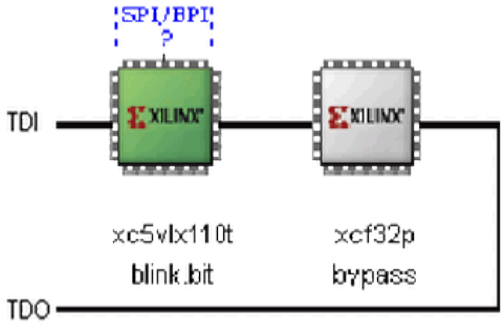
Signals	Function	FPGA#
TCL out	TDM Clock	E13
TDA in/out	TDM Data	F13

4.7 FPGA Programming

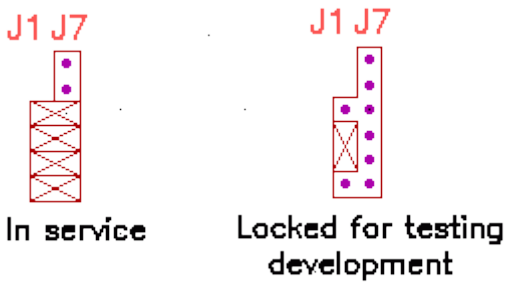
Three configuration methods are available on MHCMOD to upload (program) the FPGA core.

4.7.1 Programming through JTAG

The FPGA core can be loaded directly through the JTAG port (designated as J7 on-board) as shown in the figure below

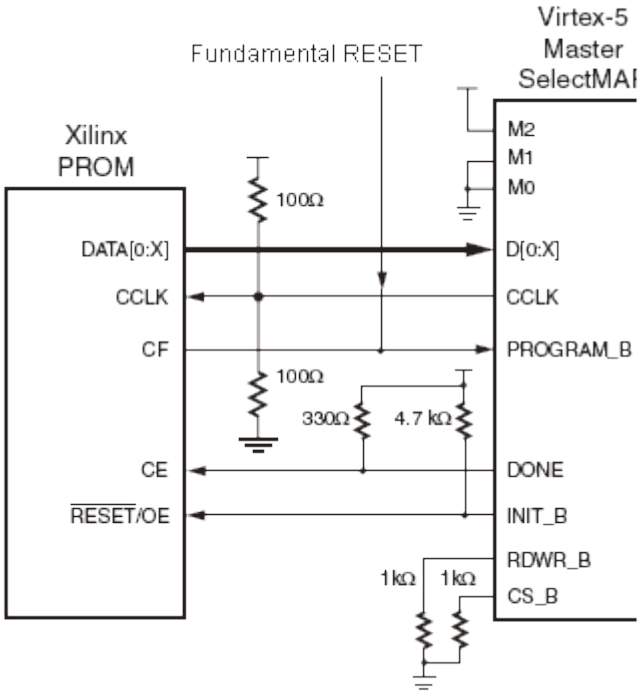


The module can be chained into board level JTAG using jumpers (J1,J7) as shown in the figure below.



4.7.2 Programming from FLASH

From the Platform FLASH (designated as U11), the FPGA can be loaded automatically.
If J4 jumper is open - it happens one time during the power-up.
If J4 is closed, every fundamental reset causes reconfiguration of the FPGA from the Platform FLASH.
The FLASH itself has to be burned through the JTAG with a valid configuration stream.



4.7.3 Partial reconfiguration

If the Platform FLASH contains the proper core implementing a PCI Express endpoint, and a controller core for ICAP (Internal Configuration Access Port) - this RESIDENT core allows the Partial reconfiguration of the FPGA.
TRANSIENT cores can be loaded that way.

J6 jumper controls HSWAPEN.

4.8 Status LEDs

There are two status LEDs assigned to a MHC module.
One red colored MFAULT (Module Fault or alarms) and one green colored MACT (Module Activity). The table below summarizes the assignment:

Signal	LED	FPGA#
MACT	Green	H15
MFAULT	Red	G15

5. COREx - Interface controllers

5.1 Overview

COREA is a 44-Pin High-Performance dual SFP line interface module controller based on PIC18F45J10 from Microchip. COREC is the single counterpart for XFP modules.

Ten blocks of module receptacles available on CBOARD designated as PA1,PB1,...PJ1.
Each block has its own COREx controller loaded with individual firmware designated as COREA,COREB,...COREJ, and commenced from the MHC using serial communication lines.
Dual SFP's use COREA type controllers, since XFP modules use COREC.

5.2 Module control commands and status

There are two major types of communication implemented in COREx, unicast, and broadast.

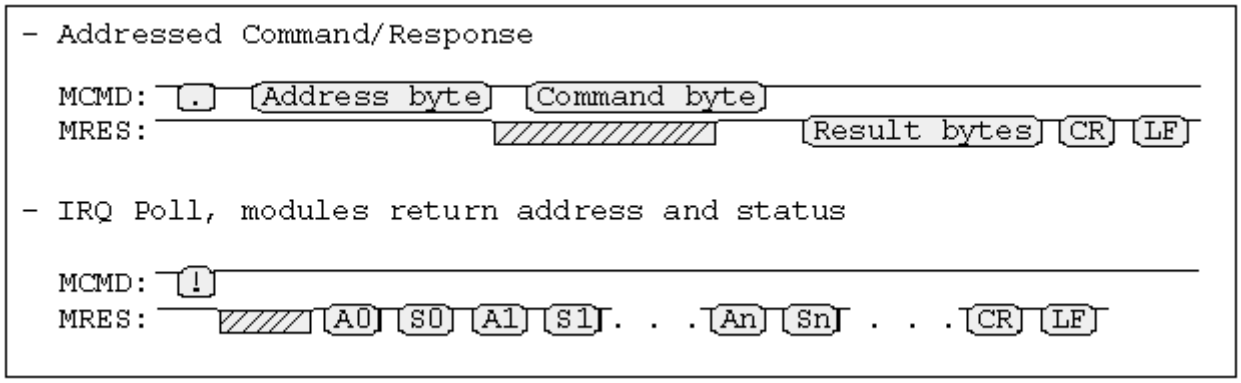
In case of unicast communication MHC sends 0x2E (period), followed by the address of the designated module. Interface 0 is addressed by 0x30 (ASCII zero character), 1 is 0x31, etc. . .

The next byte can be a command, or a query as shown below. Controllers do not echo back the MCMD characters, just interpret them.

Once a controller is addressed and start executing the command/query, all others release the MRES bus, and start snooping the activity on it upon the active unit returns results. Once idle state detected, all units become online again.

Broadcast is used to bring all units up at once, and request IRQ status, etc...

The next figure shows the timing of the command/response protocol.



The command set and descriptions are summarized below:

Mnemonic	CodeASCII	Description
MOD_RST	0x7E ~	Reset
MQRY_AD0	0x30 0	Returns AD0 value
MQRY_AD1	0x31 1	Returns AD1 value
MQRY_AD2	0x32 2	Returns AD2 value
MQRY_AD3	0x33 3	Returns AD3 value
MOD_AON	0x41 A	Activity LED On
MOD_CON	0x43 C	C port to high
MOD_EON	0x45 E	E port to high
MOD_FON	0x46 F	Fault LED On
MQRY_LONG	0x49 I	Module Details
MOD_AOFF	0x61 a	Activity LED Off
MOD_COFF	0x63 c	C port to low
MOD_DEG	0x64 d	Degraded rate
MOD_EOFF	0x65 e	E port to low
MOD_FOFF	0x66 f	Fault LED Off
MQRY_IDN	0x69 i	Module ID
MOD_LON	0x6C l	Laser on
MQRY_MAC	0x6D m	Returns MAC address
MOD_NOR	0x6E n	Normal rate
MOD_LOFF	0x6F o	Laser off
MOD_PON	0x70 p	Power on
MOD_POFF	0x71 q	Power off
MQRY_STA	0x73 s	Returns Module Status
MOD_HOST	0x74 t	Takeover (host)
MOD_AUTO	0x75 u	Automatic up
MQRY_VER	0x76 v	Returns FW version
MOD_DOWN	0x78 x	Takeover and down

Note:
s,**u**,**x** and ~ commands can also be broadcasted

The status bits arrangement, and the corresponding defineants:

Bit	7	6	5	4	3	2	1	0
	AUTO	1	DEG	FAULT	LOS	TX	POWER	PLUG

Mnemonic	CodeASCII	Description
MSTA_EMPTY	0x40 @	Empty
MSTA_DOWN	0x41 A	Administrative down
MSTA_TESTING	0x43 C	Admin testing
MSTA_UP	0x47 G	Admin up and Go
MSTA_UP_FAULT	0x57 W	Up but faulted
MSTA_UP_DEGRADED	0x67 g	Admin up degraded
MSTA_UP_DEGFAULT	0x77 w	Degraded, Faulted
MSTA_LOS	0x4F O	LOS alarm but up
MSTA_UP_LOSF	0x5F _	LOS+Fault
MSTA_UP_LOSD	0x6F o	LOS+RATS
MSTA_UP_LOSFD	0x7F [DEL]	. . . bricked

The API header *MODCMD.H* containing defineants for C programming language is enclosed in Appendix B.3.

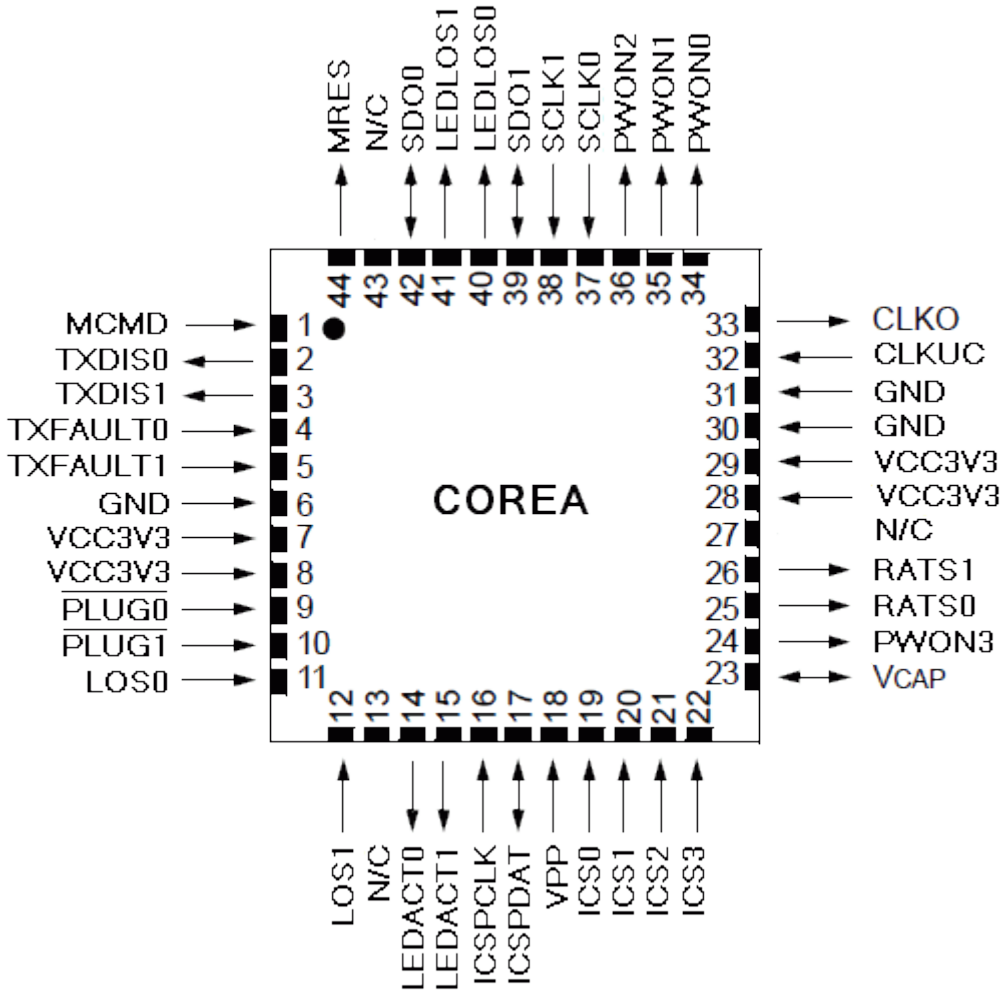
5.3 CBOARD power grid

Other application of COREx is to control and monitor the power grid of CBOARD. The following tables contains the switch/current sensor positions and routing.

Control point (CTRL) consists of the COREx designator (A...J), and the switch A/D pairs ID (0..3). Next columns contain power on, and off commands, since the last one shows the designated CBOARD target.

CTRL	ON	OFF	Target
A0	0p	0q	Interface 0, SFP lower cage
A1	1p	1q	Interface 1, SFP upper cage
A2	0C	0c	K: DRR2 RAM 1.8V
A3	0e	0E	K: Core 1V
B0	2p	2q	Interface 2, SFP lower cage
B1	3p	3q	Interface 3, SFP upper cage
B2	2C	2c	K: GT transceivers 1.2V
C0,1,2	4p	4q	Interface 4, XFP all rails
C2			PEG current measurement
C3			COM express measurement
D0	5p	5q	Interface 5, SFP lower cage
D1	6p	6q	Interface 6, SFP upper cage
D2	5C	5c	N: DRR2 RAM 1.8V
E0	7p	7q	Interface 7, SFP lower cage
E1	8p	8q	Interface 8, SFP upper cage
E2	7C	7c	N: GT transceivers 1.2V
F0	9p	9q	Interface 9, SFP lower cage
F1	:p	:q	Interface 10, SFP upper cage
F2	9C	9c	L: GT transceivers 1.2V
F3			N: DDR3 RAM current
G0	;p	;q	Interface 11, SFP lower cage
G1	<p	<q	Interface 12, SFP upper cage
G2	;C	;c	L: DRR2 RAM 1.8V
G3	;e	;E	L: Core 1V
H0,1,2	=p	=q	Interface 13, XFP all rails
I0	>p	>q	Interface 14, SFP lower cage
I1	?p	?q	Interface 15, SFP upper cage
I2	>C	>c	M: GT transceivers 1.2V
I3	>e	>E	N: Core 1V
J0	@p	@q	Interface 16, SFP lower cage
J1	Ap	Aq	Interface 17, SFP upper cage
J2	@C	@c	M: DRR2 RAM 1.8V
J3	@e	@E	M: Core 1V

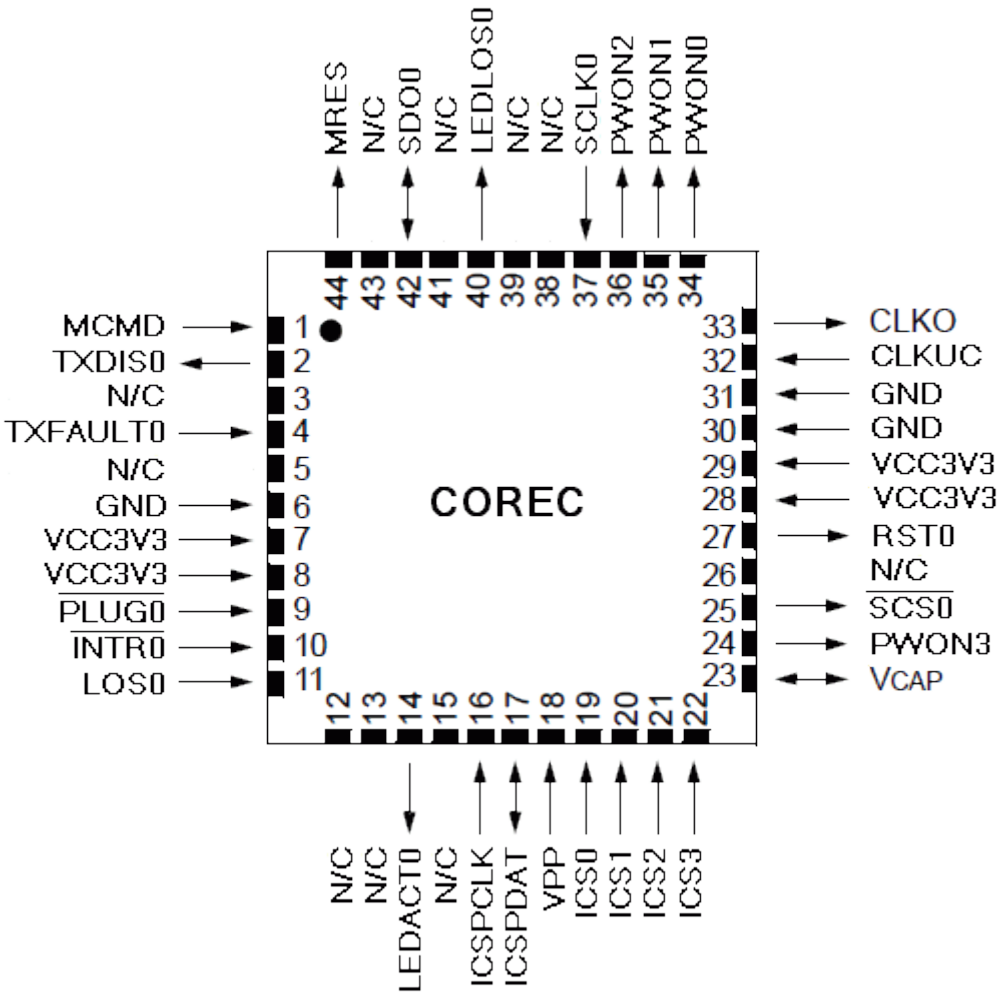
5.4 COREA pinout and description



Pin name	Pin number	Type	Description
CLKUC	32	Input	24 MHz clock input
CLKO	33	Output	Clock output
MCMD	1	Input	Module command from MHC (115200,8,N,1)
MRES	44	Tristate	Module response
ICSPCLK	16	Input	In system programming clock
ICSPDAT	17	In/Out	In system programming data
VPP	18	Power	In system programming voltage
GND	6,30,31	Power	Power return (ground)
VCC3V3	7,8,28,29	Power	Power voltage, 3.3V nominal
ICS0..3	19..22	Analog input	Current sensors (A/D inputs)
PWON2,3	36,24	Output	Auxiliary power comtrol
SFP 0 (lower cage) signals			
LEDACT0	14	Output	Activity LED output (green)
LEDLOS0	40	Output	Alarm LED output (red)
TXDIS0	2	Output	Disable transmission (laser off)
TXFAULT0	4	Input	Transmitter fault condition
PLUG0	9	Input bar	SFP module present (low)
LOS0	11	Input	Loss Of Signal alarm
RATS0	25	Output	Full bandwidth
PWON0	34	Output	Power on (3.3 V supply)

SCLK0	37	Output	IIC clock (module definition)
SDO0	42	In/Out	IIC data (module definition)
SFP 1 (upper cage) signals			
LEDACT1	15	Output	Activity LED output (green)
LEDLOS1	41	Output	Alarm LED output (red)
TXDIS1	3	Output	Disable transmission (laser off)
TXFAULT1	5	Input	Transmitter fault condition
PLUG1	10	Input bar	SFP module present (low)
LOS1	12	Input	Loss Of Signal alarm
RATS1	26	Output	Full bandwidth
PWON1	35	Output	Power on (3.3 V supply)
SCLK1	38	Output	IIC clock (module definition)
SDO1	39	In/Out	IIC data (module definition)

5.5 COREC pinout and description



Pin name	Pin number	Type	Description
CLKUC	32	Input	24 MHz clock input
CLKO	33	Output	Clock output
MCMD	1	Input	Module command from MHC (115200,8,N,1)
MRES	44	Tristate	Module response
ICSPCLK	16	Input	In system programming clock
ICSPDAT	17	In/Out	In system programming data

VPP	18	Power	In system programming voltage
GND	6,30,31	Power	Power return (ground)
VCC3V3	7,8,28,29	Power	Power voltage, 3.3V nominal
ICS0..3	19..22	Analog input	Current sensors (A/D inputs)
PWON3	24	Output	Auxiliary power comtrol
XFP signals			
LEDACT0	14	Output	Activity LED output (green)
LEDLOS0	40	Output	Alarm LED output (red)
TXDIS0	2	Output	Disable transmission (laser off)
TXFAULT0	4	Input	Transmitter fault condition
PLUG0	9	Input bar	XFP module present (low)
LOS0	11	Input	Loss Of Signal alarm
SCS0	25	Output bar	Chip select
PWON0	34	Output	Power on (1.8 V supply)
PWON1	35	Output	Power on (3.3 V supply)
PWON2	36	Output	Power on (5 V supply)
SCLK0	37	Output	IIC clock (module definition)
SDO0	42	In/Out	IIC data (module definition)
INTR0	10	Input bar	XFP interrupt
RST0	27	Output	XFP reset/power down